

SERVICE MANUAL

2031 DISK DRIVE

HIGH AND LOW PROFILE MODELS

DEC. 1985

PN-314011-01





Computer Systems Division
1200 Wilson Drive
West Chester, PA 19380

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Commodore Business Machines, Inc.

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2031 DISK DRIVE PRODUCT SPECIFICATION

GENERAL DESCRIPTION

The 2031 is a single drive, 5-1/4 inch floppy, disk unit. It uses a 35 track, 48 TPI, single headed drive:

High profile — Shugart drive assembly

Low profile — Alps drive assembly

It is an intelligent device, containing its own microprocessor, RAM, ROM and operating systems software.

MAXIMUM STORAGE

170K of data (formatted) — 35 tracks

MEDIA

5-1/4 inch floppy disk. Single sided, single density, soft sector (double density can be used, but not needed).

INPUT/OUTPUT

IEEE interface

CONTROLLER

MOS 6502 microprocessor — 1 MHz clock

MEMORY

2K RAM, 16K ROM

DATA TRANSFER RATE

Internal 40K Bytes/sec

IEEE-488 Bus 1.2K Bytes/sec

FILE TYPES

Program, sequential, relative, random-access and user

COMPUTERS

PET, 4000 series, 8000 series, B128

MEDIA COMPATIBILITY

1541, 4040

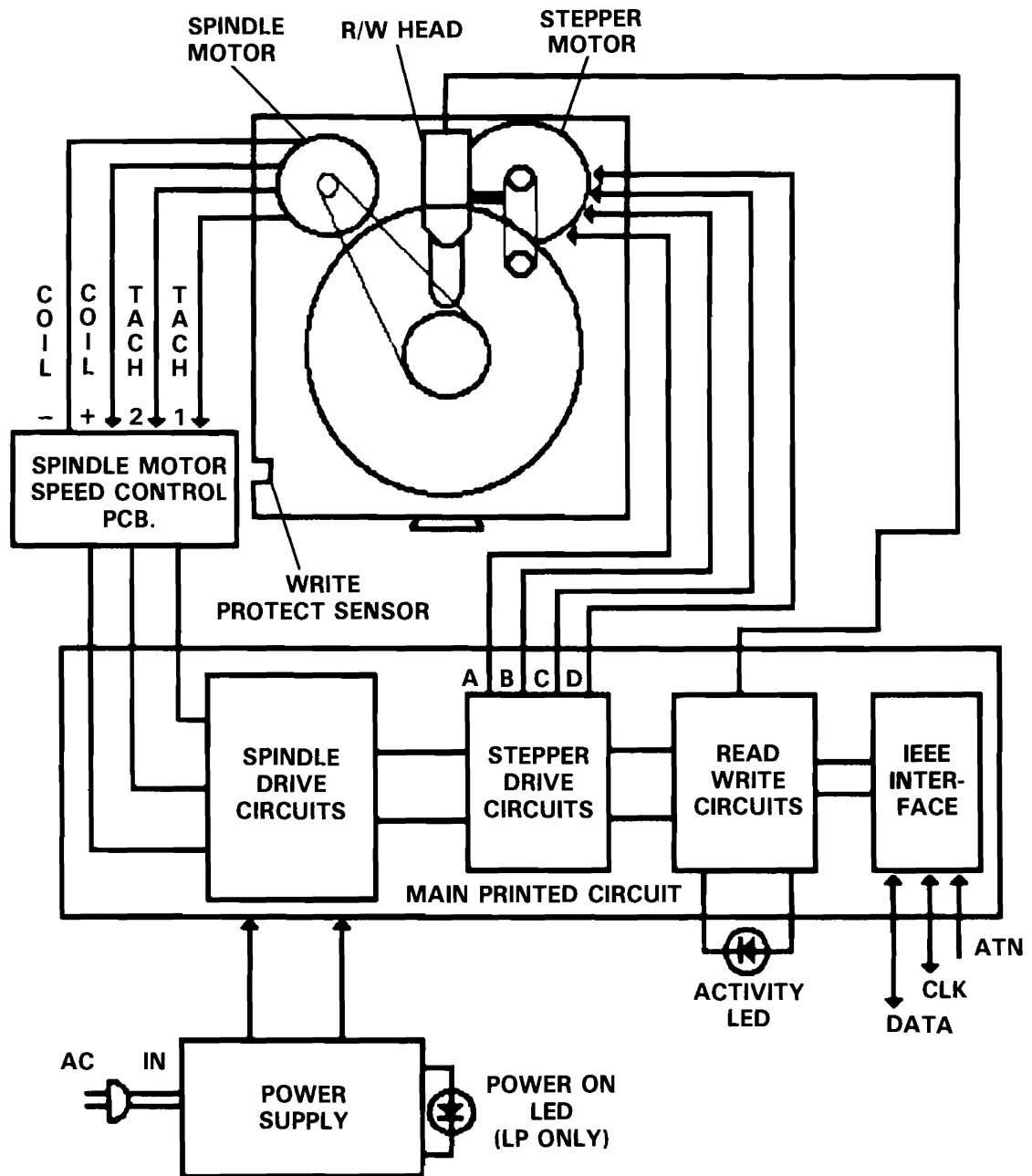
POWER REQUIREMENTS

120 Volts AC, 60Hz — integral power supply with external 1 Amp fuse

POWER CONSUMPTION

40 Watts maximum

BLOCK DIAGRAM



CARE AND MAINTENANCE

- DO NOT use MAGNETIZED tools when repairing or adjusting a disk drive.
- DO NOT place a disk drive near any device which generates "noise" e.g., — motors, radios, televisions.
- DO NOT stack drives upon each other or in any way inhibit air flow around the unit. HEAT BUILD-UP can cause disk failures.
- Periodically CLEAN the read/write head with 90% isopropyl alcohol and a cotton swab. CHECK load pad for excess wear. Clean or replace as necessary.
- Take the following precautions when handling a diskette:
 - ALWAYS store a diskette in its jacket.
 - Use ONLY felt-tip pens when writing on the label of a diskette.
 - Do not bend or physically damage a diskette.
 - Do not place a diskette in the area of a magnetic field.
 - Do not attempt to clean a diskette.
 - Do not touch the exposed area of a diskette.

DIAGNOSTIC and ADJUSTMENT procedures for the 2031 are outlined in detail in the Version 3.0 diagnostic package (Commodore Part #31405201). This Kit contains a manual that outlines testing, adjustment and alignment procedures and Version 3.0 and 3.5 diagnostic program disks.

DEVICE NUMBER CHANGE

The 2031 drive is shipped from the factory set for device #8. The channel may be hardware altered to device #9, 10 or 11. Channel selection is changed on the main logic board by LIFTING the diodes at locations CR 17/18 and/or CR 19. The following chart indicates the selected device #:

ADDRESS	LOW PROFILE	HIGH PROFILE
9	CR 19	CR 19
10	CR 17	CR 18
11	CR 19 & 17	CR 19 & 18

The diode locations are indicated on the appropriate schematic.

OVERVIEW

The drive is itself an independent memory device. The drive is composed of a media clamp rotating mechanism, a head positioning mechanism and an eject mechanism. All positioning operations, excluding insertion and removal of the diskette, are controlled by the internal guide mechanism. Closing the front door causes the media clamp mechanism to operate. Two operations are performed in the following order:

- a) The diskette is centered.
- b) The diskette is clamped and retained between the spindle and the hub.

The spindle and hub rotate at 300 r.p.m. through a closed-loop control circuit employing a D.C. motor/tachometer. It is important that the relationship between the head and the media is maintained correctly during operation. For this purpose, a pressure pad is used to hold and press down the media (about 12g) from the opposite side of the head. This head assembly is coupled to a four phase stepping motor which performs the track positioning. One step of the stepping motor corresponds to a 1/2 track movement. The control circuit on the logic board selects the direction and number of steps to the desired track.

The Read/Write head uses a glass-bonded, ferrite/ceramic head. Track-to-track erasing is accomplished by the straddle erase method. The surface of the Read/Write head is mirror-ground to minimize wear of the head and media. Also, the head is designed in such a way that the maximum signal can be obtained from the media surface.

The spindle drive motor operates on 12VDC and turns the spindle, through a belt drive, at 300 revolutions per minute. The speed of the drive motor is controlled by a feedback signal from a tachometer, which is housed in the drive motor assembly. The feedback signal controls a servo amp that supplies the 12VDC drive current.

FLASH CODE

The 2031, upon power-up, goes through its own internal diagnostic. If an electronic problem is detected, it is indicated by a FLASH CODE. The LED's will blink a set number of times, pause, and then flash again until the problem is corrected.

Number of Flashes	Possible Failure
1	Zero Page
2, 3	DOS ROM's
4	RAM

Circuitry associated with these components can also cause the failure code. Therefore, it should be suspected as the next possible defect.

CASEWORK/ACCESSORY PARTS LIST

2031 LOW PROFILE (PLASTIC CASEWORK)

2031 TOP CASE (IVORY)	C 1540014-05
1540/41/2031 BOTTOM CASE (IVORY)	C 1540015-00
SHIELD COVER	1540013-01
LED ASSEMBLY	1540003-01
SELF ADHESIVE FOOT	C 950150-02
POWER CORD.....	C 903508-04
USER'S MANUAL	C 1540042-01

2031 HIGH PROFILE (METAL CASEWORK)

REPLACEMENT CASEWORK FOR METAL UNITS IS NO LONGER AVAILABLE.

POWER CORD	C 903501-01
USER'S MANUAL	C 2031036-01
DEMO DISKETTE	C 1540041-01
IEEE TO IEEE INTERFACE CABLES	C 905080-01
PET TO IEEE INTERFACE CABLES	C 320101-01

TROUBLESHOOTING GUIDE

NOTE: Always check for latest ROM/ECO upgrade. If socketed IC is suspected bad, be sure to check socket with ohmmeter.

SYMPTOM:	POSSIBLE SOLUTION:
No LED's on power up.	Is Power cord plugged into wall outlet correctly? Is Power cord plugged into the disk drive correctly? Check line fuse. Check power switch. Check clock on 6502 pin 37. Check +5 and +12 volt lines.
Error LED flashes on power up.	Check all RAM and ROM locations.
Error LED stays on all the time.	Check 6502 microprocessor. Check ROMs.
Drive motor runs continuously and red LED stays on.	Check +12V. Check 6502, logic gates.
Drive motor runs continuously and red LED stays off.	Check ROM Check drive motor PCB.
Drive motor runs continuously.	Check VR2 (5V Regulator). Check Power Transformer.
After the drive warms up the motor runs continuously.	Check 6522s. Check motor control PCB.
Loads programs with red LED flashing.	Check drive speed. Check stepper motor.
Loading is intermittent.	Check ROMs. Check drive alignment.
Does not load when hot or LED flashed 3 times.	Check ROMs.
Searches with LED flashing continuously.	Check ROMs.
Searching with no red LED.	Check 6522s, logic gates.
Message of 'FILE NOT FOUND' is displayed.	Clean drive head w/alcohol. Check Ø stop adjustment. Check alignment.
Drive fails to read.	Check the 311, 9602, and 592s. There are two +12 volt sources for stepper output and read circuit, make sure both are good.

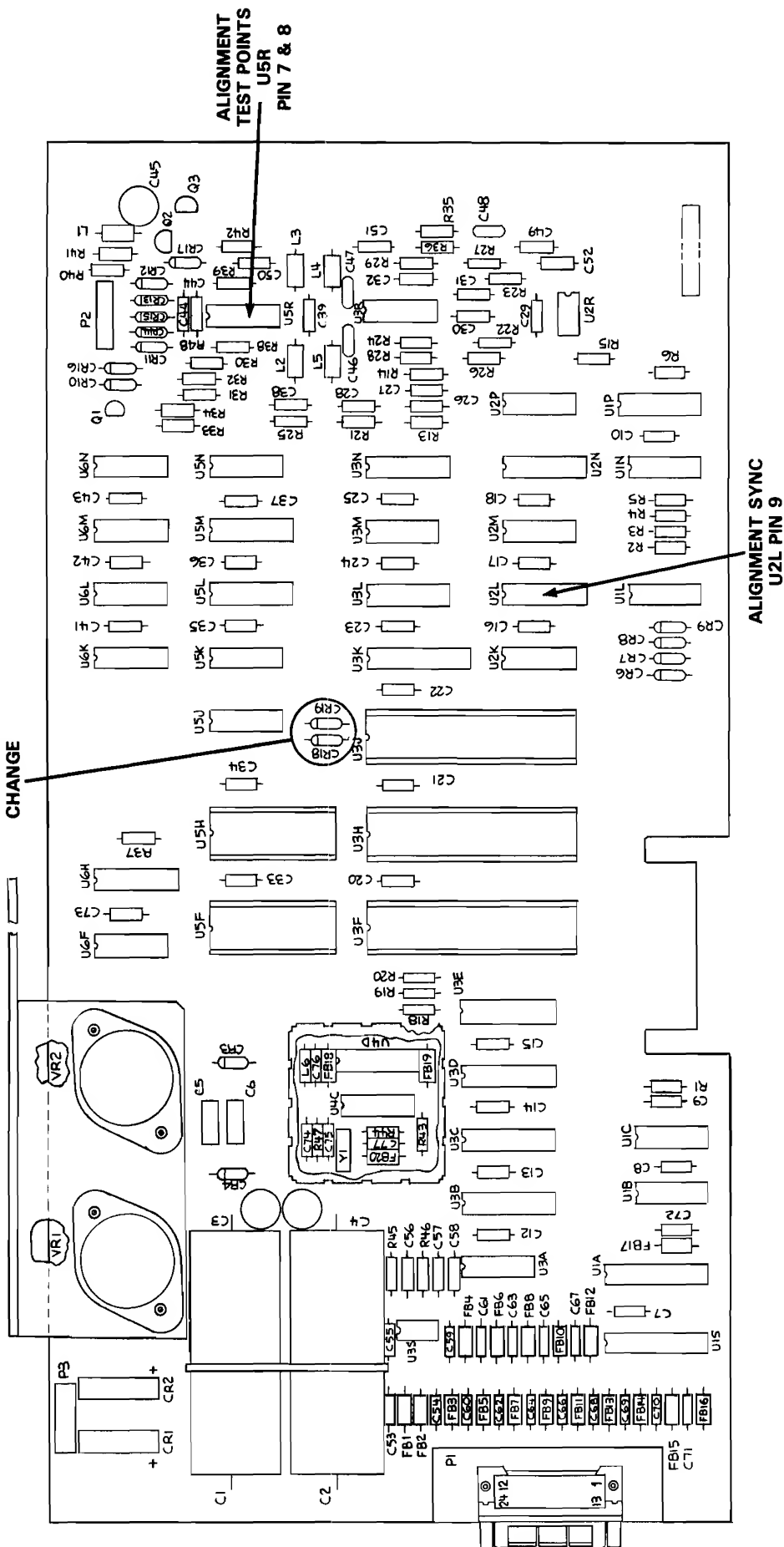
TROUBLESHOOTING GUIDE (Continued)

SYMPTOM:	POSSIBLE SOLUTION:
Fails to format disk.	Check components related to connector P7. Check 6522s. Check write circuits.
Stepper Motor does not step forward.	Check 6502, 6522s, stepper logic.
Drive speed will not stabilize.	Check DC motor.
Will not save when the drive heats up.	Check 6502 microprocessor.
Locks-up when loading.	Check IEEE interface components. Check ROM.
Fails the performance test and displays a 21 read error.	Check test diskette. Check Drive Motor.
Fails the performance test and displays a 27 read error.	Check stop adjust.
Passes performance test to track 18 then displays 21 read errors.	Check read/write head.
Passes the performance test but will not load certain programs.	Check stepper motor.

HIGH PROFILE

PCB ASSEMBLY #2031040 BOARD LAYOUT

DEVICE #
CHANGE



PARTS LIST

PCB ASSEMBLY #2031040-01

PLEASE NOTE:

Commodore part numbers are provided for reference only and do not indicate the availability of parts from Commodore. Industry standard parts (Resistors, Capacitors, Connectors) should be secured locally. Approved cross-references for TTL chips, Transistors, etc. are available in manual form through the Service Department, order part #314000-01. Unique or non-standard parts will be stocked by Commodore and are indicated on the parts list by a "C". Vendor Name and part number have been provided for your convenience in ordering custom or unique parts.

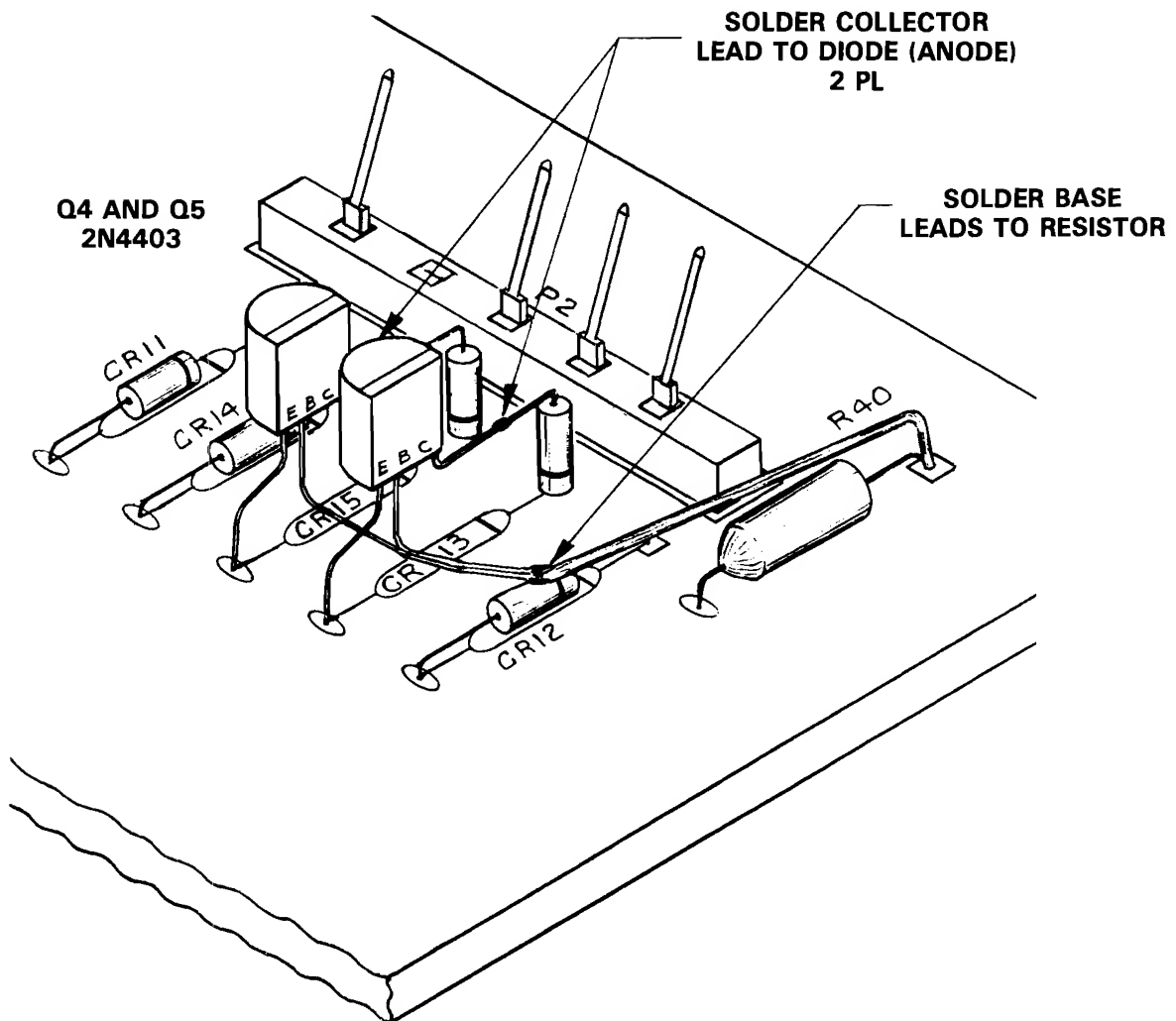
INTEGRATED CIRCUITS			RESISTORS — All Values are in ohms- 1/4 W 5% unless noted otherwise.			
U1A	75161 Transceiver	901494-01	R1	2K	R31,32	1.5K
U1B	74LS14	901521-30	R2-5	150	R33	1K
U1C	7406	901522-06	R6	680	R34	680
U1N	7406	901522-06	R13	5.1K	R35,36	220
U1P	74LS139	901521-18	R14	330	R37	2K
U1S	75160 Transceiver	901493-01	R15	510	R38,39	9.09K, 1/4 W, 1%
U2K	74LS164	901521-28	R18-20	2K	R40	1K
U2L	74LS133	901521-15	R21	22K	R41	180
U2M	74LS02	901521-21	R22,23	470	R42	270
U2N	74LS193	901521-26	R24	430	R43	47
U2P	74LS86	901521-32	R25	330	R44	2.2K
U2R	311 OP Amp	901523-04	R26,27	2.2K	R45,46	1M
U3A	74LS04	901521-02	R28,29	150	R47	4.7K
U3B,C,D,E	2114 Static RAM	901453-04	R30	300	R48	6.19K, 1/4 W, 1%
U3F	6502 Microprocessor	C 901435-01	CAPACITORS			
U3H	6522	C 901437-01	C1,2	Low Leak Elect	4700µF	25V
U3J	6522	C 901437-01	C3,4	Low Leak Elect	47µF	16V
U3K	74LS245	901521-46	C5,C6	Low Leak Elect	1µF	50V
U3L	74LS165	901521-12	C7-10	Ceramic	.1µF	50V
U3M	74LS74	901521-06	C12-18	Ceramic	.1µF	50V
U3N	9602 One Shot	901510-01	C20-25	Ceramic	.1µF	50V
U3R	592	901523-08	C26	Ceramic	22pF	50V
U3S	555 Timer	901523-01	C27	Ceramic	750 pF	50V
U4C	7400	901522-04	C28,29	Ceramic	330 pF	50V
U4D	74LS193	901521-26	C30,31	Ceramic	.022µF	50V
U5F	2364 ROM	C 901484-05	C32	Ceramic	1000 pF	50V
U5H	2364 ROM	C 901484-03	C33-37	Ceramic	.1µF	50V
U5J	74LS04	901521-02	C38,39	Ceramic	750 pF	50V
U5K	74LS00	901521-01	C41-44	Ceramic	.1µF	50V
U5L	74LS191	901521-40	C45	Low Leak Elect	10µF	25V
U5M	74LS193	901521-26	C46,47	Low Leak Elect	.47µF	50V
U5N	74LS74	901521-06	C48	Tantalum	3.3µF	35V
U5R	592	901523-08	C49-52	Ceramic	.1µF	50V
U6F	74LS04	901521-02	C53-54	Ceramic	47 pF	
U6H	74LS42	901521-17	C55,56	Ceramic	.1µF	50V
U6K	74LS10	901521-24	C57	Ceramic	1.0µF	50V
U6L	74LS04	901521-02	C58	Ceramic	.01µF	50V
U6M	74LS00	901521-01	C59-71	Ceramic	47 pF	
U6N	7406	901522-06	C72,73	Ceramic	.1µF	50V
TRANSISTORS			C74	Ceramic	100 pF	
Q1	2N4401		C75	Ceramic	220 pF	
Q2	2N4400		C76	Ceramic	.047µF	
Q3,4,5	2N4403		C77	Ceramic	47 pF	
DIODES			MISCELLANEOUS			
CR1	1.5 A, 50V, Bridge Rectifier	900756-01	P1	RT Angle CNNCT IEEE	903206-01	
CR2	4 A, 200V, Bridge Rectifier	900755-01	P2	Header — R/W Head CNNCT		
CR3,4	1N4005		P3	Header — PWR CNNCT		
CR6-9	1N4005		L1-3	Choke 100µH		
CR10	1N5231, 5.1 V Zener		L4,5	Choke 22µH		
CR11-16	1N4148		L6	Inductor 2.2µH		
CR17	1N5226B, 13.3 V Zener		VR1	Voltage Regulator LM323		
CR18,19	Germanium 1N270		VR2	Voltage Regulator LM340		
			Y1	Crystal 16 MHz	900556-02	
				Shield Box	4022048-01	
				Shield Cap	4022047-01	

2031 HP UPGRADE NOTES

A design error was present in the original 2031 High Profile Single Disk Drive. The write circuit was modified to correct the problem, however, it is possible that some units still need to be revised.

Revision to correct write circuit:

1. Lift Diodes, CR13 & CR15 as shown.
2. Install Transistors, solder the Collector Lead to Diodes.
3. Solder the Center Leads of Transistors together, to R40 Resistor as shown. (Use 20 AWG wire for mechanical strength.)
4. Solder Emitter Leads to feed thru.
5. Change R31 & R32 from 2.7K Ω to 1.5K Ω .



2031 HP CIRCUIT THEORY

Microprocessor/VIA Logic

U3J is a VIA, Versatile Interface Adapter. During a write operation, the microprocessor passes the data to be recorded to Port A of U3J. The data is loaded into the shift register U3L. It is converted from parallel to serial data and output to the write amplifier circuit. During a read operation, serial data is received from the read amplifier circuit.

The stepper motor is controlled by two outputs on port B of U3J, STP0, and STP1. A binary four count is developed from these two lines by U1P, see Sheet 4. The MTR output on pin 12 controls the spindle motor, refer to the motor control schematic on page 18. The write protect switch, WPS, is monitored at pin 14 of U3J and the red activity LED is controlled at pin 13.

Varying Frequency Clock

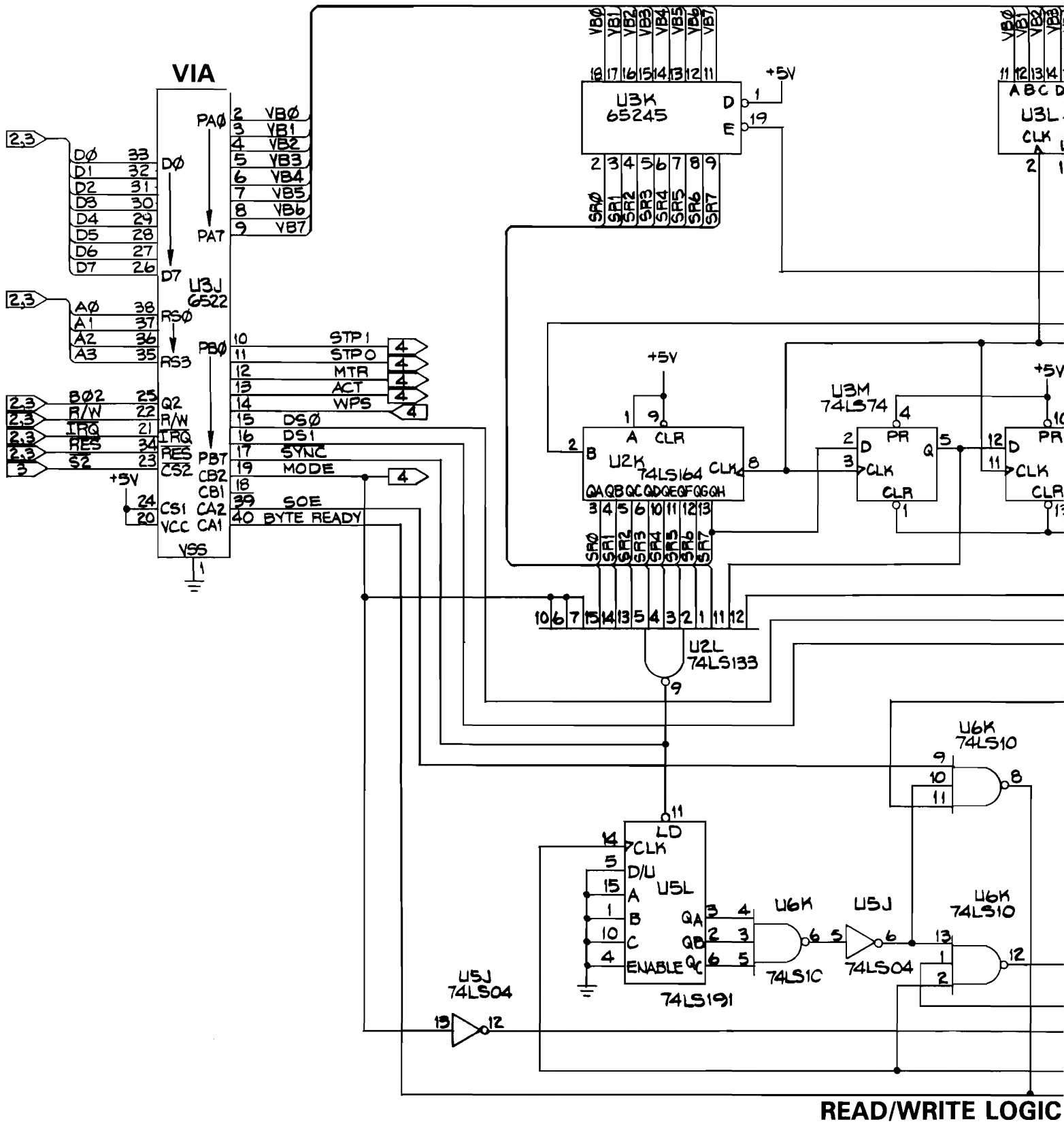
The DS0 and DS1 outputs of U3J, pins 15 and 16, are input at pins 1 and 15 of U5M. U5M is a programmable counter ($\div 16, \div 15, \div 14, \div 13$) that outputs a varying frequency clock used to compensate for the difference in recording area/sector for sectors on inner tracks (Trks 1,2,3) as compared to sectors on out most tracks (Trks 33,34,35). The area/sector for inner tracks is less than the area/sector for outer tracks, so the recording clock frequency is increased when writing on inner tracks to keep the flux density constant. This clock output is on pin 12 of U5M and is used to clock the data from the read amplifier circuits.

Tracks	Clock Frequency	Divide By
1-17	1.2307 MHz	13
18-24	1.1428 MHz	14
25-30	1.0666 MHz	15
31-35	1 MHz	16

Read/Write Control Logic

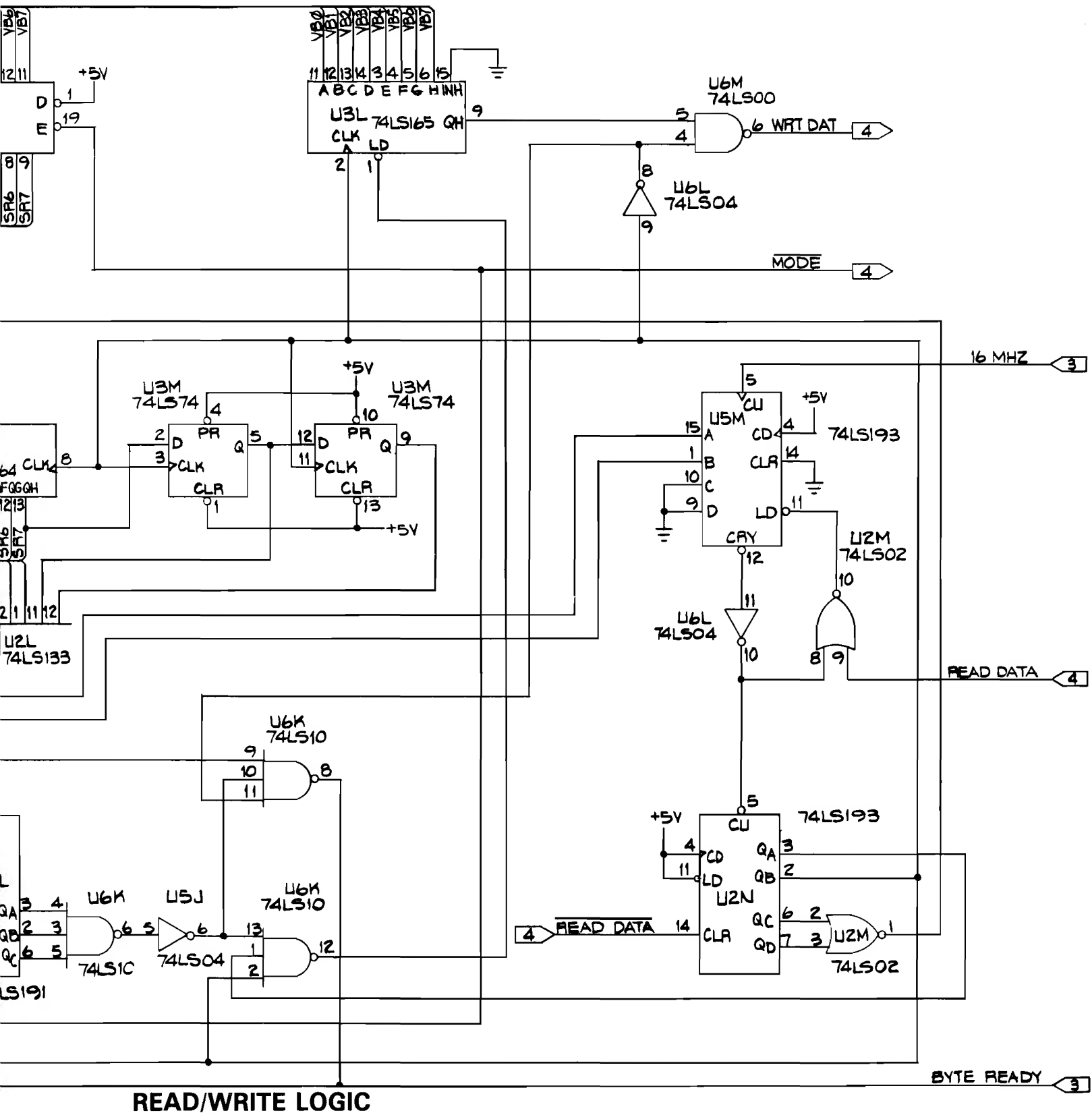
During a write operation, U3L converts parallel data into serial data. The output on pin 9 is input to 'NAND' gate U6M pin 5. U6M outputs the serial data on pin 6 at the clock rate determined by the input signal on pin 4. The output clocks the D flip flop U5N (see Sheet 4). The outputs of U5N, Q and \bar{Q} , drive the write amplifiers.

During a read operation, data from the read amplifiers is applied to the CLR input of counter U2N. The outputs, C and D, are shaped by the 'NOR' gate U2M. U2M outputs the serial data on pin 1, then it is converted to parallel data by U2K. The output of U2K is latched by U3K. The serial bits are counted by U5L. When 8 bits have been counted, U6K pin 6 goes "low", U5J pin 6 goes "high", and U6K pin 8 goes "low" indicating byte is ready to be read by the processor. U2L monitors the parallel output of U2K. When all 8 bits are "1", the output pin 9 goes "low" indicating a sync bit has been read.



SCHEMATIC 2031038

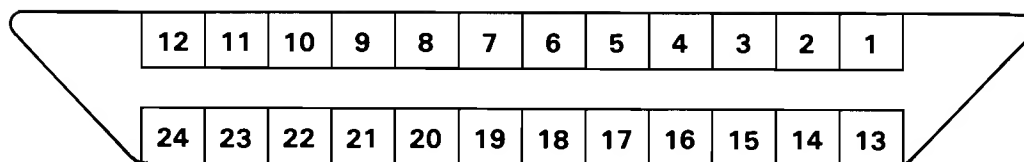
SHEET 1 of 4



READ/WRITE LOGIC

BYTE READY 3

2031 HP CIRCUIT THEORY



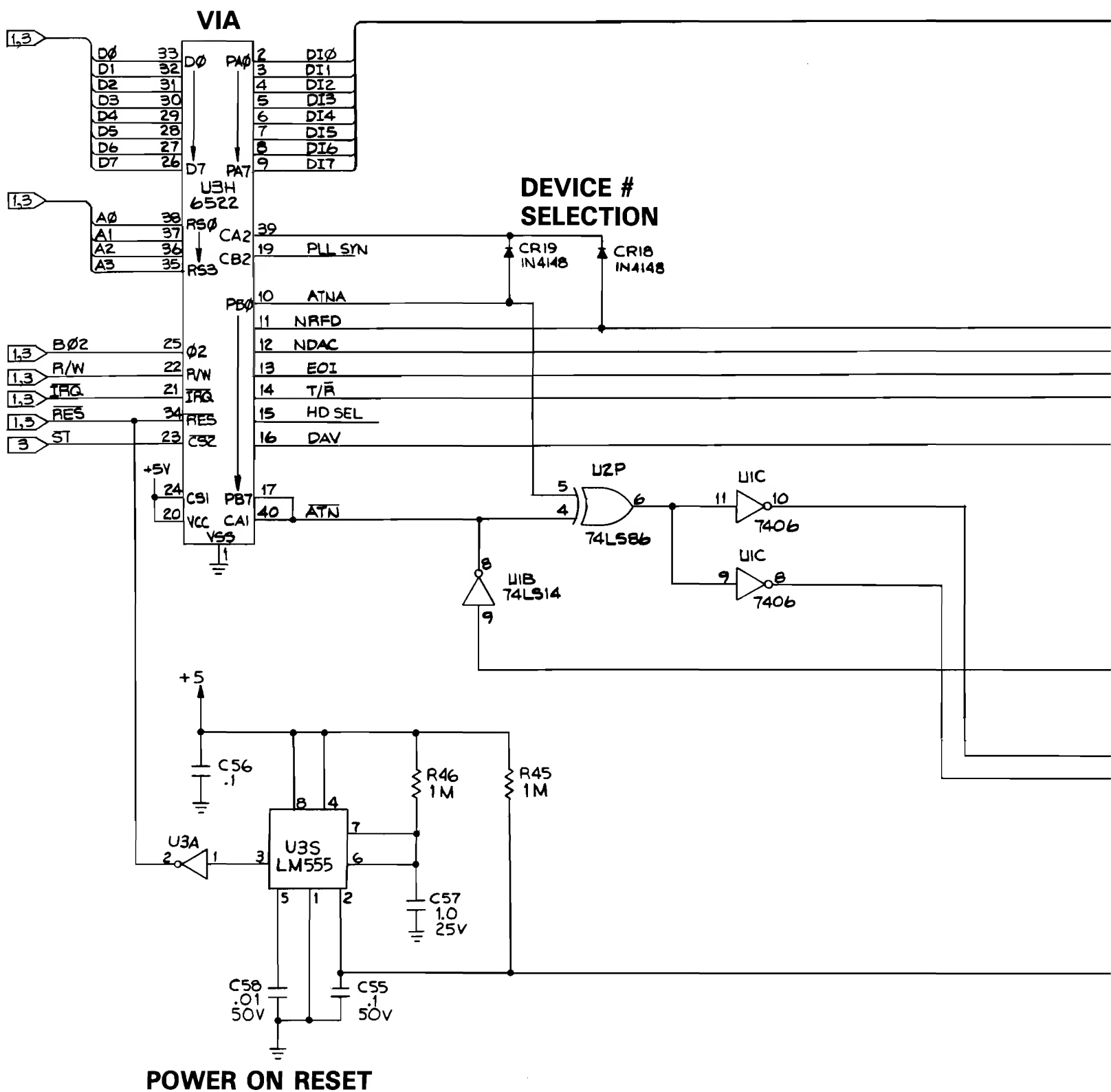
IEEE Interface

All of the signals on the interface are controlled by the I/O device U3H. Eight parallel bi-directional data lines, PA0-PA7, are used as the parallel data bus for the interface. U1S is an octal bus transceiver used to provide communication on the general purpose interface bus, GPIB, between operating units of the system. The data transfer and bus-management signals are communicated by U1A, thus completing the 16-line interface of the IEEE-488 bus.

DAV	Data Valid	DAV low signifies data is valid on the data bus.
EOI	End or Identify	CBM always sets EOI low while the last data byte is being transferred.
DAC	Data Not Accepted	DAC is low when data is being read and returned high after the last data byte is read.
RFD	Not Ready For Data	RFD is low until all receivers are ready to accept data, then the line will go high.
SRQ	Service Request	Not implemented in BASIC but available to the CBM user.
ATN	Attention	The host sets the signal low while sending commands on the data bus.
REN	Remote Enable	REN is held low by the bus controller and the host has this pin permanently grounded.
IFC	Interface Clear	The host sends its internal reset signal as IFC low to initialize all devices.

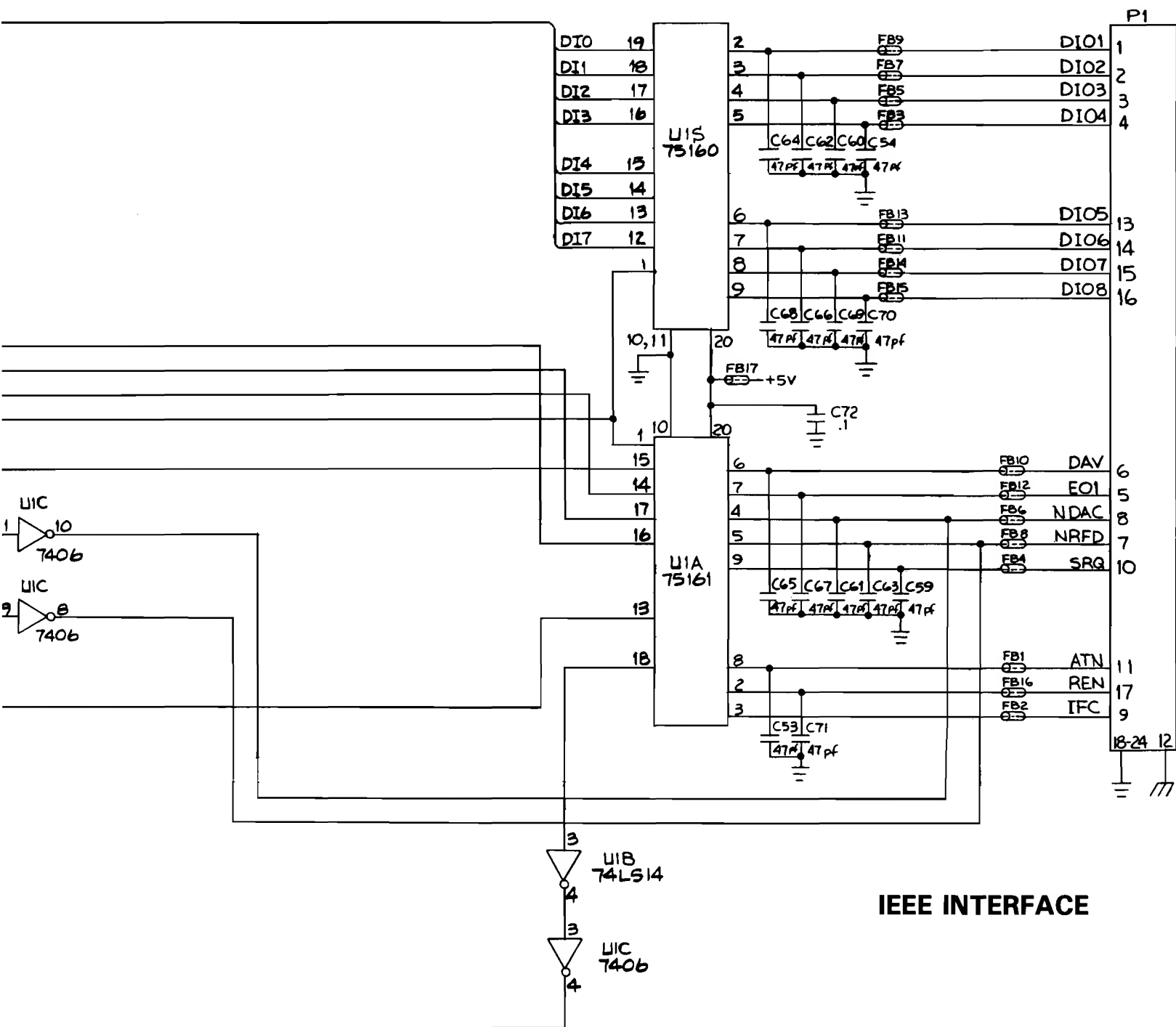
Reset Logic

The 2031 disk drive is automatically reset on power up by U3S, a 555 timer, when triggered by the 5V applied at pin 8. A reset can also be set by the IFC line on the IEEE interface. The output pulse width is determined by the values of R43 and C36. The pulse width = $1.1 \times R43 \times C36 \approx 1$ second. The output on pin 3 of U3S is an active "high". It is inverted by U3A to active "low". A low output at U3A pin 2, resets the unit and initializes all of the microprocessor logic.



SCHEMATIC 2031038

SHEET 2 of 4



2031 HP CIRCUIT THEORY

Microprocessor Control of RAM and ROM

U5F and U5H are 8192 x 8 bit ROMS that store the Disk Operating System (DOS). U5F resides at memory locations \$C000-\$DFFF. U5H resides at memory locations \$E000-\$FFFF. U5J and U5K decode the addresses output from the microprocessor when selecting these ROMS.

U3B, C, D and E are 2114 Static RAMS (24 x 4). They reside at memory locations \$0000-\$07FF. This memory is used for processor stack operations, general processor housekeeping, user program storage, and 4 temporary buffer areas. U5J, U5K, and U6J decode the addresses output from the processor when selecting RAM. U6J also decodes the address selection of the VIAs, U3J and U3H.

The Clock Circuit

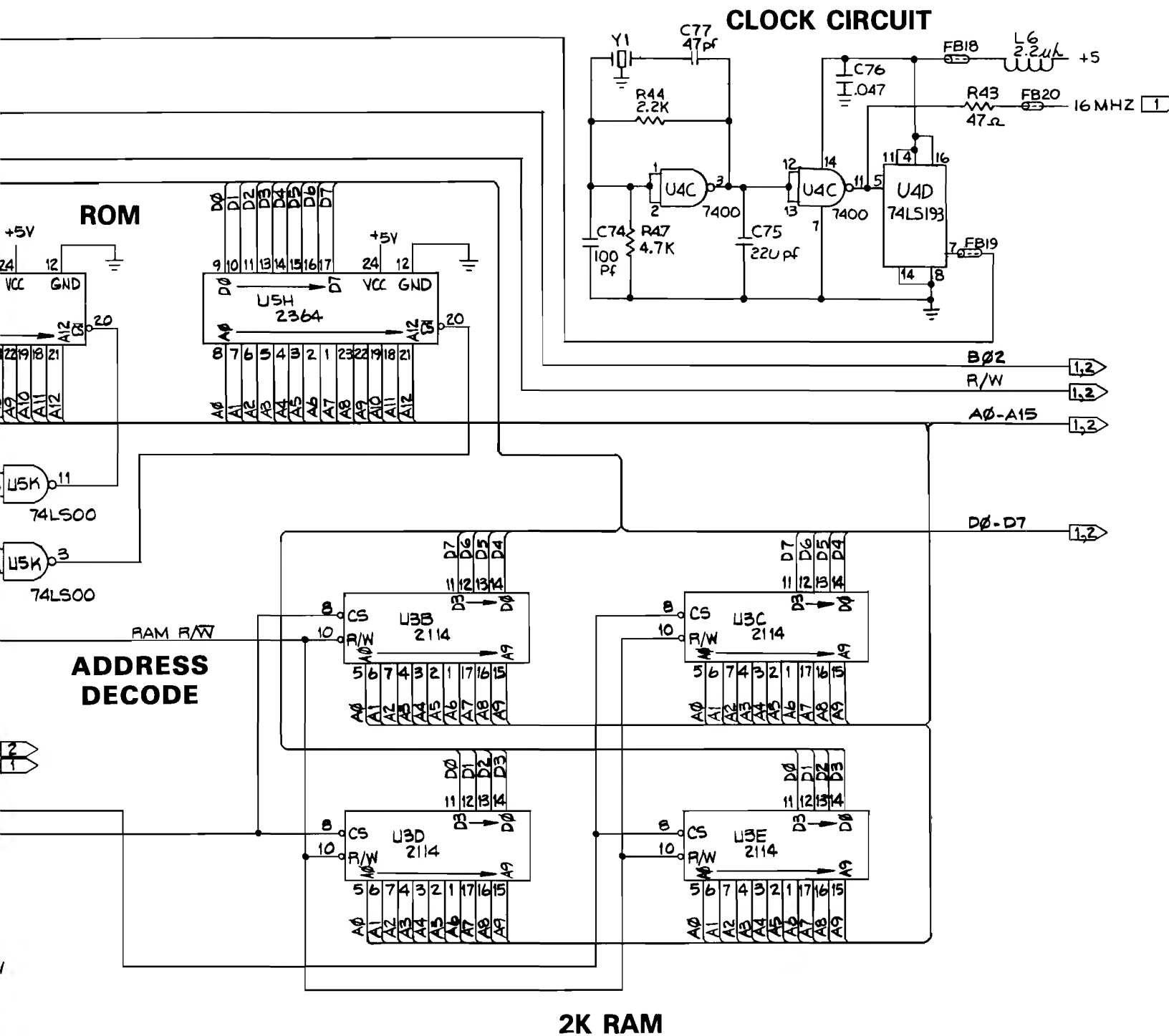
The clock circuit outputs a 16 MHz clock signal at U4C pin 11. This is input to U4D on pin 5. U4D is configured as a $\div 16$ frequency divider. The output of U4D pin 7 is a 1 MHz clock signal used as the system clock (Phase 0) for the microprocessor. The 16 MHz clock signal is also used for the varying frequency clock circuit, see Sheet 1.

The Power Supply

THE CHASSIS: When the switch is closed, the AC voltage input is applied to the primary winding of the transformer. Circuit protection is provided by a .5 amp fuse. The transformer steps down the AC input voltage into two smaller AC voltages: One secondary output (approx. 16VRMS) is applied at connector P3 pins 1 and 4, the other secondary output (approx. 9VRMS) is applied at P3 pins 2 and 3.

THE PCB: The 16VRMS AC applied between pins 1 and 4 is converted to DC by the full wave bridge rectifier CR1. The DC output of CR1 is regulated at + 12VDC by VR2. High frequency filtering is provided by C6, low frequency filtering by C2 and C4. The 9VRMS AC applied between pins 2 and 3 is converted to DC by the full wave bridge rectifier CR2. The DC output is regulated at + 5VDC by VR1. High frequency filtering is provided by C5, low frequency filtering by C1 and C3.

[illegible]



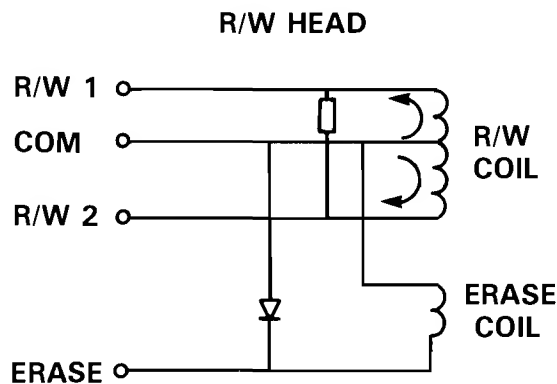
2031 HP CIRCUIT THEORY

Stepper Motor Control Circuits

U1P converts STP0 and STP1 into outputs that create a binary four count. The outputs Y0, Y1, Y2, and Y3 from U1P are inverted by U1N. The outputs of the inverters drive the transistors of U1L. The current output from these transistors drive the individual phase coils in the stepper motor and return to the 12VDC supply. CR6-CR9 suppress the CEMF developed by the motor coils.

Read Amplifier Circuits

When data is recorded on the disk, a "1" bit is represented on the disk by a change in direction of magnetic flux, caused by a change in direction of current passed through the R/W coil in the R/W head. When a "0" bit is to be recorded, no change in current flow direction occurs, causing the direction of the magnetic flux to remain the same on the disk.



When data is being read from the disk, CEMF is induced into the R/W coil by the magnetic fields on the disk, causing current flow which is detected by the read amplifiers. Current flow through the R/W coil will forward bias either CR12 or CR14, depending on the direction. Q1 and CR16 must be forward biased. The first amplifier, U5R, senses this current flow from the R/W coil on one of the inputs and amplifies it. L2, L3, L4, L5 and C39 act as a low pass filter, suppressing noise on the amplified output. U3R is a differential amplifier which amplifies the difference of the two input signals from the filter section. U2R is a peak detector. The output of U2R will pulse "high" when a "1" is read. This signal is the reconstruction of data recorded. The time domain filter, U3N, times out when a "1" bit has been read, so unwanted "1" bits are not added to the actual data. The one shot, U3N, generates the correct data pulse width.

Write Amplifier Circuits

During a write operation, pin 4 of U6N must be "high". This forward biases Q1 and CR16. If pin 5 of U5N, Q, goes "low", Q4 and CR15 become forward biased, passing current flow through R/W 1. If \bar{Q} goes "low", Q5 and CR13 become forward biased, passing current flow through R/W 2.

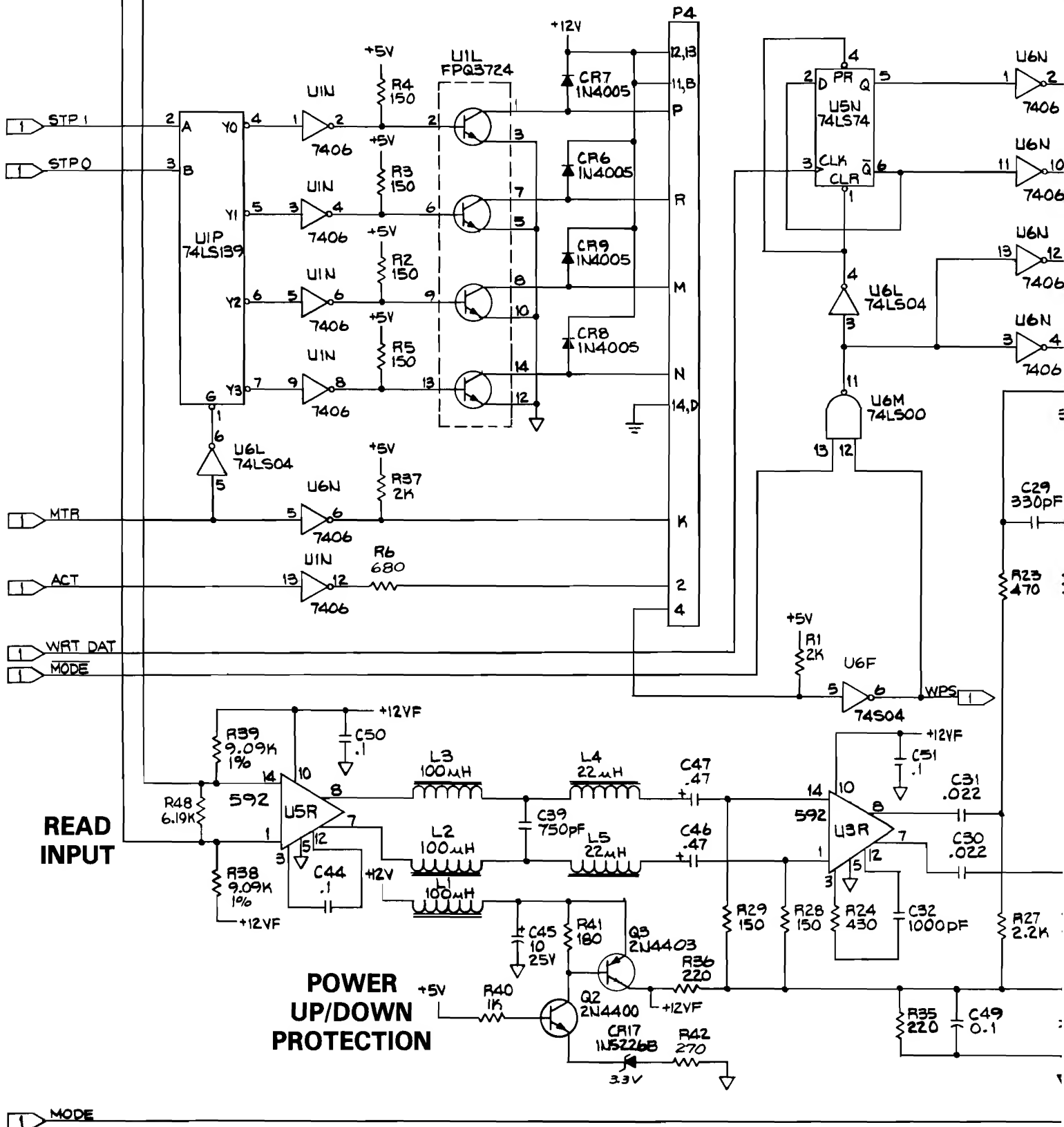
When a write operation occurs, the ERASE coil is energized by forward biasing CR11. This demagnetizes the outer edges of the track, preventing data on one track from bleeding into the next track.

Power Up/Down Write Protection

This circuit prevents erroneous data from being written on the disk during power up/down sequences. During a power up, the 12VDC supply is not applied to the R/W coils and amplifier circuits before the processor has control of the logic. During a power down, the 12VDC supply is removed from the R/W coils and amplifier circuits before the processor loses control of the logic.

Q3 acts as a series pass transistor biased to regulate the 12VF output to the R/W coils and amplifier circuits. Q2 is a feedback amplifier monitoring the 5VDC supply. CR17 develops a precise reference voltage for Q2. L1 and C45 delay the 12VDC supply.

STEPPER MOTOR



SHEET 4 of 4

2031 HP POWER SUPPLY ASSEMBLY PARTS LIST

FUSE HOLDER

ROCKER SWITCH

904507-01

POWER CONNECT FILTER

903467-03

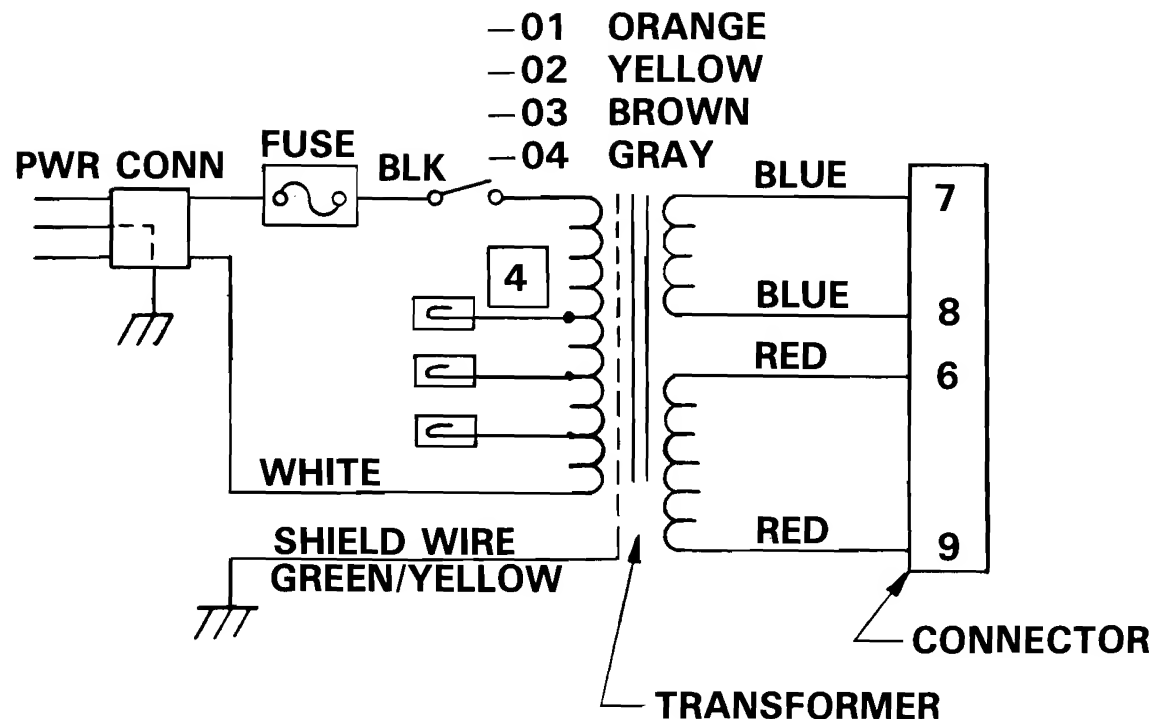
FUSE, SLOW BLO, 250V, .5A

903555-15

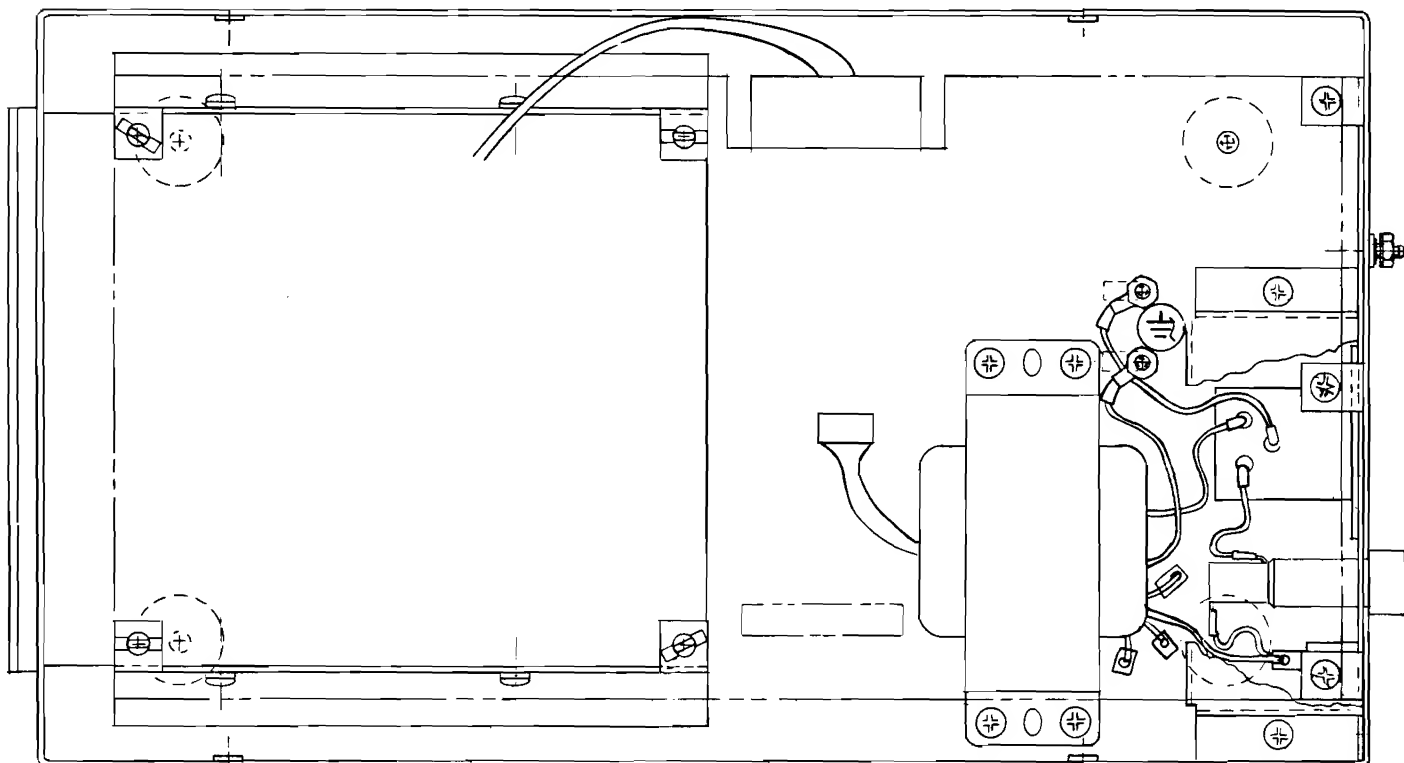
POWER TRANSFORMER

320939-01

2031 HIGH PROFILE POWER SUPPLY #2031002-01



WIRING DIAGRAM



ASSEMBLY DRAWING

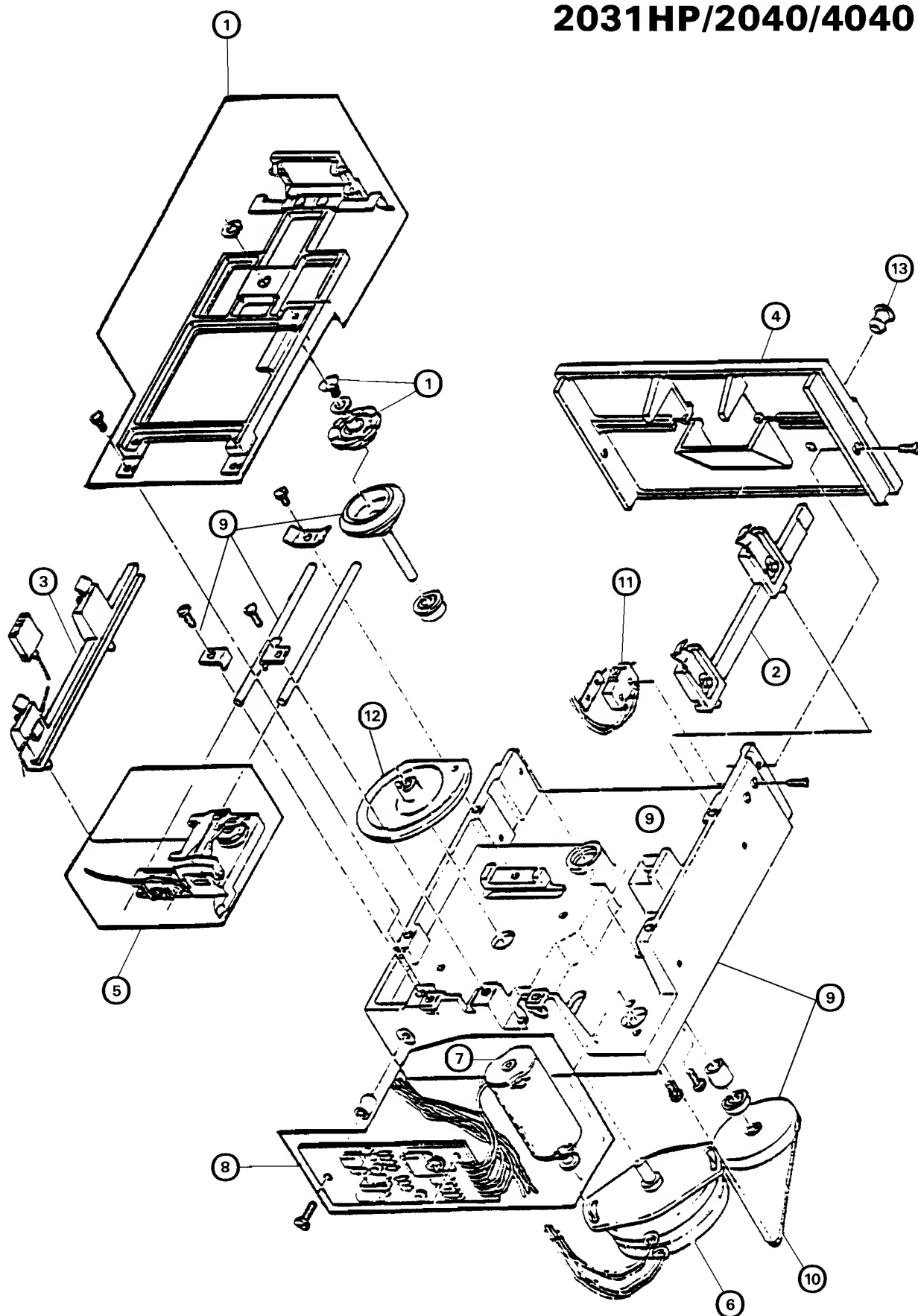
PARTS LIST

95055000 Shugart Drive Assembly

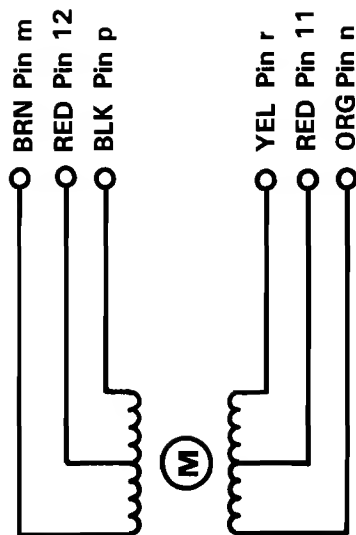
- ① 31414001 SHU DOOR/HUB ASSEMBLY
1-Door Assy w/Frame
2-Hub/Collet Assy
- ② 31414101 SHU LEFT DISK GUIDE
- ③ 31414201 SHU RIGHT DISK GUIDE
- ④ 31414301 SHU FRONT BEZEL
- ⑤ 31414401 SHU R/W HEAD ASSEMBLY
1-R/W Head w/Harness
2-Load Arm w/Pad
- ⑥ 31414501 SHU STEPPER MOTOR ASSEMBLY
1-Stepper Motor w/Harness
- ⑦ 31414601 SHU D.C. MOTOR
- ⑧ 31414701 SHU MOTOR CONTROL PCB
- ⑨ 31414801 SHU HOUSING/SPINDLE ASSY
1-Housing Base
2-Spindle Assy
3-L/R Guide Shafts
- ⑩ 31414901 SHU DRIVE BELT
- ⑪ 31415001 SHU WRITE PROTECT SWITCH

31415101 SHU HARDWARE
1-Assorted Screws
- ⑫ 31415201 SHU CAM ACTIVATOR
- ⑬ 903820-03 UNIV. LAMP HOLDER SET

SHUGART DRIVE ASSEMBLY 2031HP/2040/4040

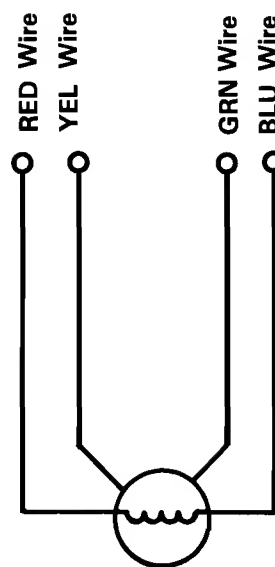


RESISTANCE CHECKS HIGH PROFILE — SHUGART DRIVE



Stepper Motor

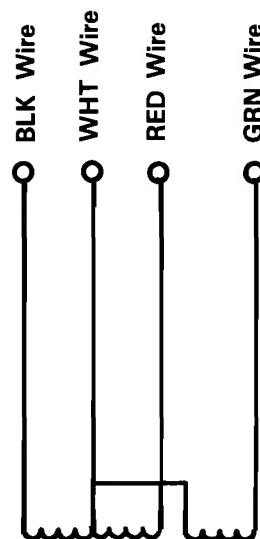
End to end on either coil = 74 ohms
End to centertap = 37 ohms



Spindle Motor

Motor coil (red wire to blue wire) = 71 ohms
Tach coil (green wire to yellow wire) = 175 ohms at rest
Tach coil while rotating spindle = 135 — 195 ohms

Measurements made at connector on motor control pcb.



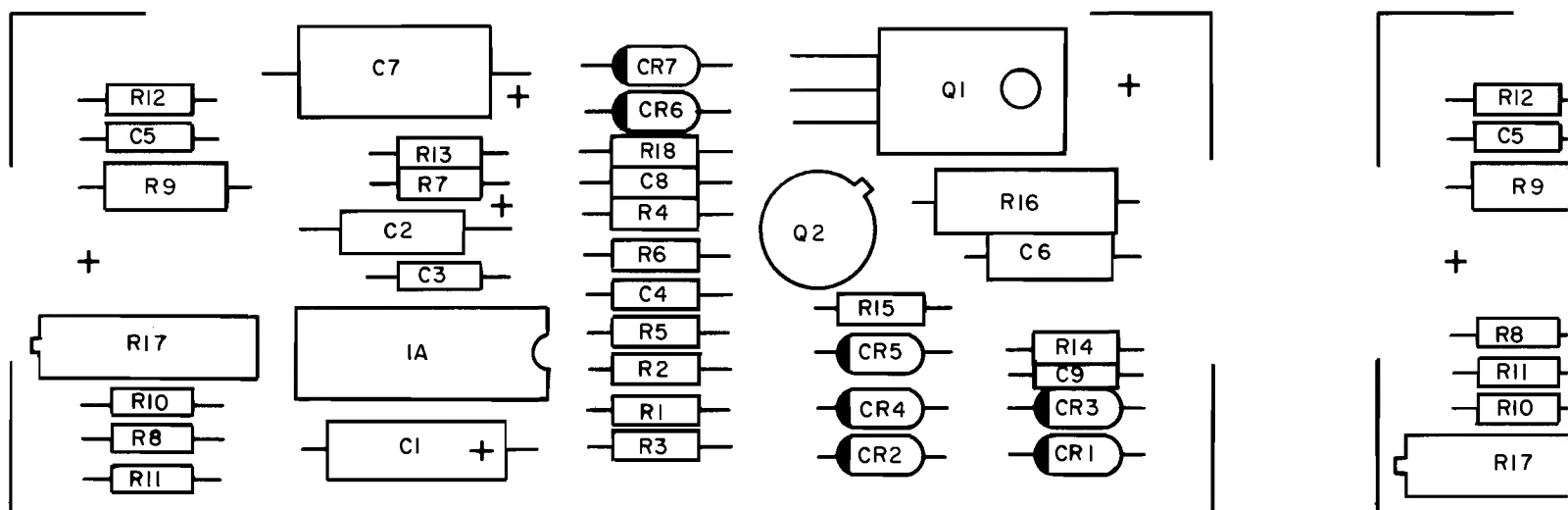
R/W Head

R/W coil (black wire to red wire) = 28.5 ohms
R/W coil (red wire to white wire) = 15 ohms
R/W coil (black wire to white wire) = 15 ohms
Erase coil (green wire to white wire) = 11.9 ohms

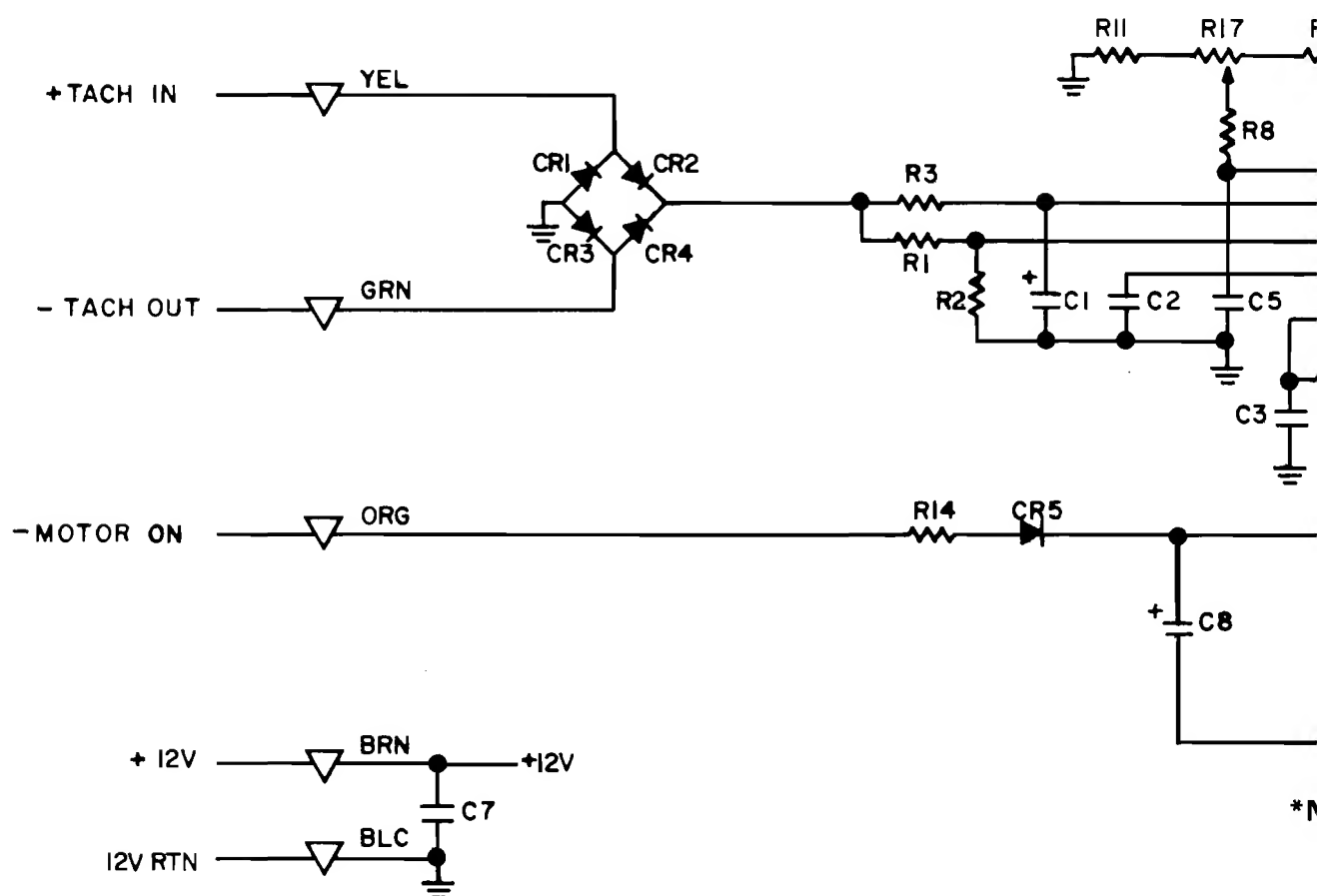
Measurements made at the 5 pin plug at the end of the R/W head cable.
The plug should be disconnected.

PARTS LIST

INTERGRATED CIRCUITS		
1A	LM 2917N	
TRANSISTORS		
Q1 Q2	GE 7941 sub: GE 7947 M10060-0	
DIODES		
CR1-7	IN4148	
CAPACITORS — All values in microfarads		
C1	4.7	50V Tant
C2	.015	35V 5%
C3	.047	50V
C4	.47	50V Tant
C5	.1	50V
C6	1	35V
C7	220	16V Elect
C8	.47	50V Tant
C9	.015	50V (Assy 25181 ONLY)
RESISTORS — Ceramic 1/8W All values in ohms at 5% unless otherwise noted		
R1	100	1%, 1/8W
R2	909	1%, 1/8W
R3	10K	
R4	4.7K	
R5	40.2K	1%, 1/8W
R6	160K	
R7	12	
R8	27K	
R9	470	
R10	23.2K	1%, 1/8W
R11	7.5K	1%, 1/8W
R12	68	
R13	68	
R14	2K	
R15	150	
R16	.68,	5%, 1W
R17	5K	Trim Pot Rectangle, 3/4 in.
R18	20K	

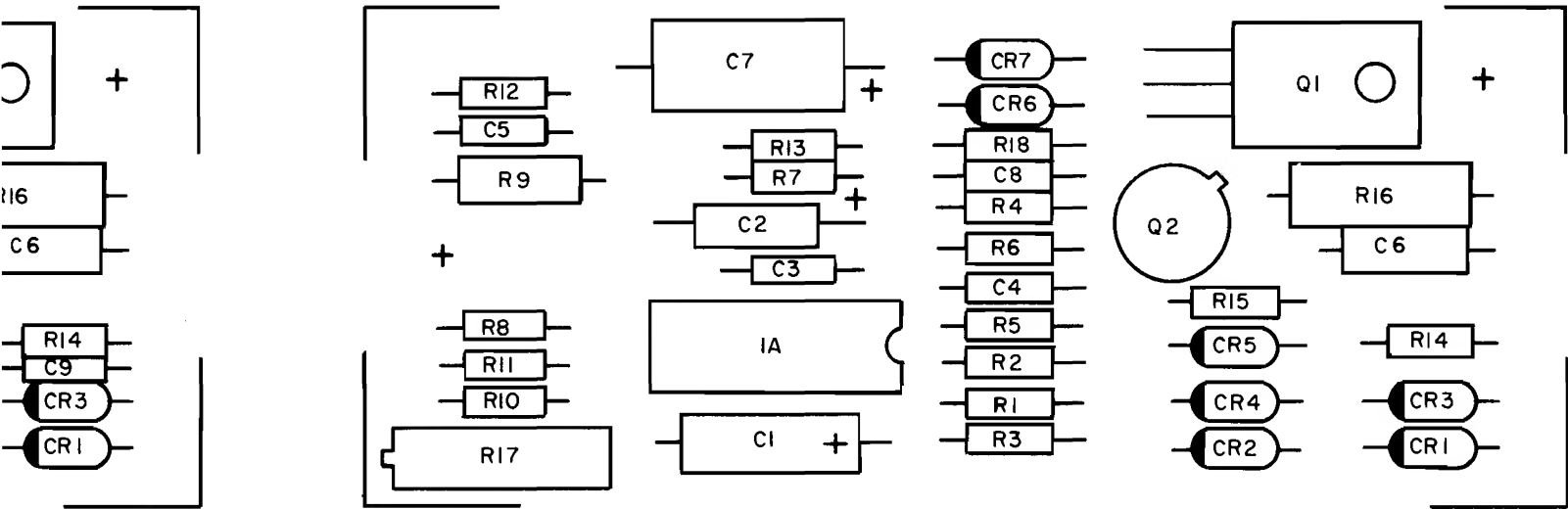


COMPONENT LOCATIONS
MOTOR CONTROL PCB ASSEMBLY P/N 25181

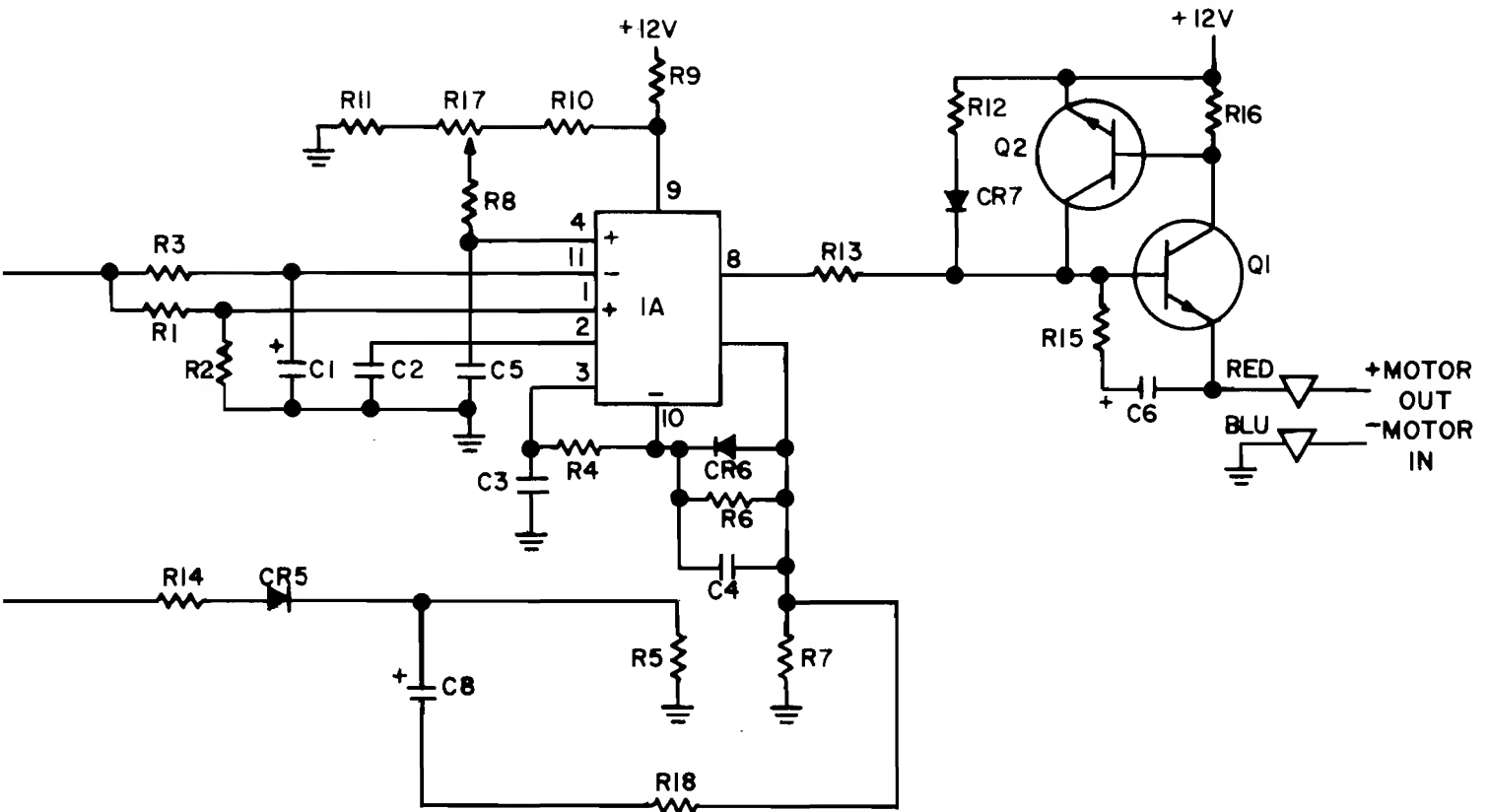


SCHEMATIC

SHUGART SERVO BOARD (COMMODORE PART #31414701)



COMPONENT LOCATIONS
MOTOR CONTROL PCB ASSEMBLY P/N 25129



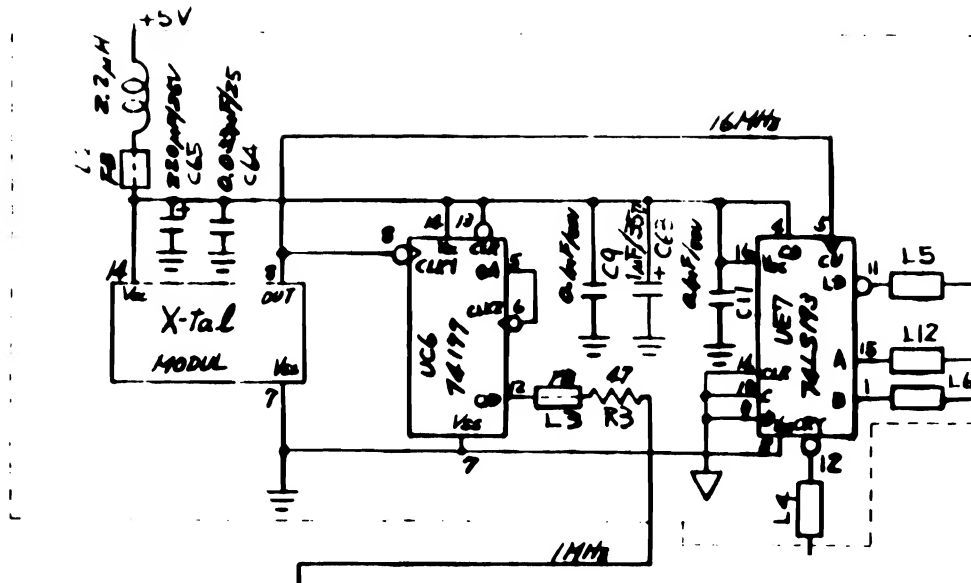
*NOTE: ASSEMBLY P/N 25181
INCLUDES C9 ON
COLLECTOR OF Q1.

SCHEMATIC

LOW PROFILE

[illegible]

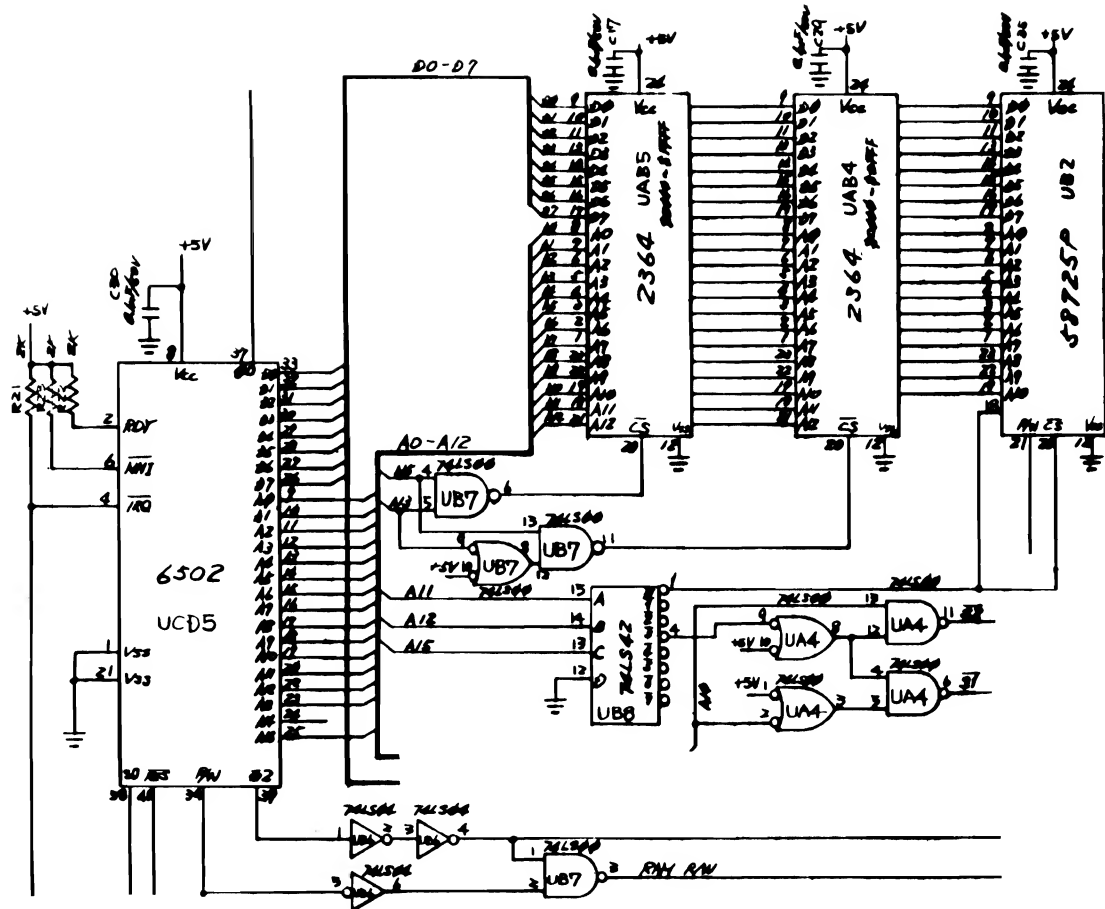
2031 LP CIRCUIT THEORY



The Clock Circuits

Crystal Y1 outputs a 16 MHz clock signal. This is input to UC6 on pin 8. UC6 is configured as a $\div 16$ frequency divider. The output of UC6 pin 12 is a 1 MHz clock signal used as the system clock (Phase 0) for the microprocessor. UE7 is a programmable counter ($\div 16$, $\div 15$, $\div 14$, $\div 13$) that outputs a varying frequency clock used to compensate for difference in recording area/sector for sectors on inner tracks (Trks 1,2,3) as compared to sectors on out most tracks (Trks 33,34,35). The area/sector for inner tracks is less than the area/sector for out most tracks, so the recording clock frequency is increased when writing on inner tracks to keep the flux density constant. This clock output is on pin 12 of UE7.

Tracks	Clock Frequency	Divide By
1-17	1.2307 MHz	13
18-24	1.1428 MHz	14
25-30	1.0666 MHz	15
31-35	1 MHz	16



Microprocessor Control of RAM and ROM

UAB4 and UAB5 are 8192 x 8 bit ROMs that store the Disk Operating System (DOS). UAB4 resides at memory locations \$C000-\$DFFF. UAB5 resides at memory locations \$E000-\$FFFF. UB7 decodes the addresses output from the microprocessor when selecting these ROMs.

UB2 is a 2048 x 8 bit RAM. UB2 resides at memory locations \$0000-\$07FF. This memory is used for processor stack operations, general processor housekeeping, user program storage, and 4 temporary buffer areas. UA4, UB6, UB7 and UB8 decode the addresses output from the processor when selecting RAM.

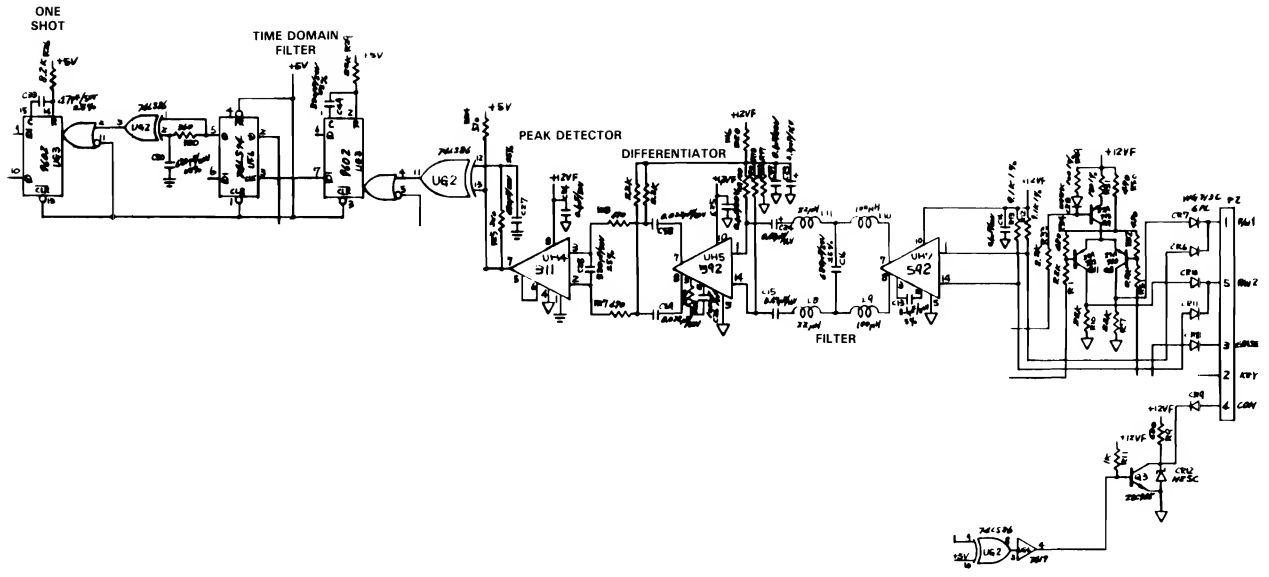
UB8 also controls the chip select line of the VIA, UCD4.



Read/Write Control Logic

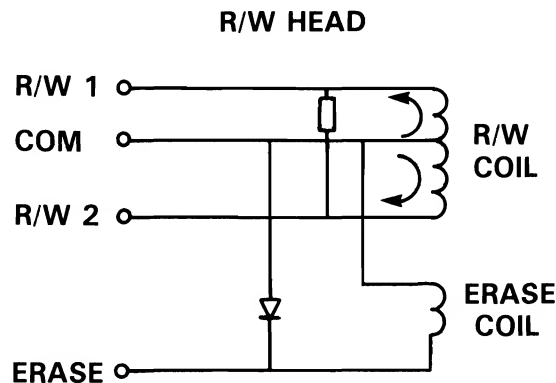
UCD4 is a VIA (Versatile Interface Adapter). During a write operation, the microprocessor passes the data to be recorded to Port A of UCD4. The data is then loaded into UD3 which converts the parallel data into serial data. The output on pin 9 is input to 'NAND' gate UF5 pin 4. UF5 outputs the serial data on pin 6 at the clock rate determined by the input signal on pin 5. The output clocks the D flip flop UF6. The outputs of UF6, Q and \overline{Q} , drive the write amplifiers.

During a read operation, data from the read amplifiers is applied to the CLR Input of counter UF4. The outputs, C and D, are shaped by the 'NOR' gate UE5. UE5 outputs the serial data on pin 1, then it is converted to parallel data by UD2. The output of UD2 is latched by UC3. The serial bits are counted by UE3, when 8 bits have been counted, UF3 pin 12 goes "low", UC1 pin 6 goes "high", and UF3 pin 8 goes "low" indicating byte is ready to be read by the processor. UC2 monitors the parallel output of UD2, when all 8 bits are "1", the output pin 9 goes "low" indicating a sync bit has been read.

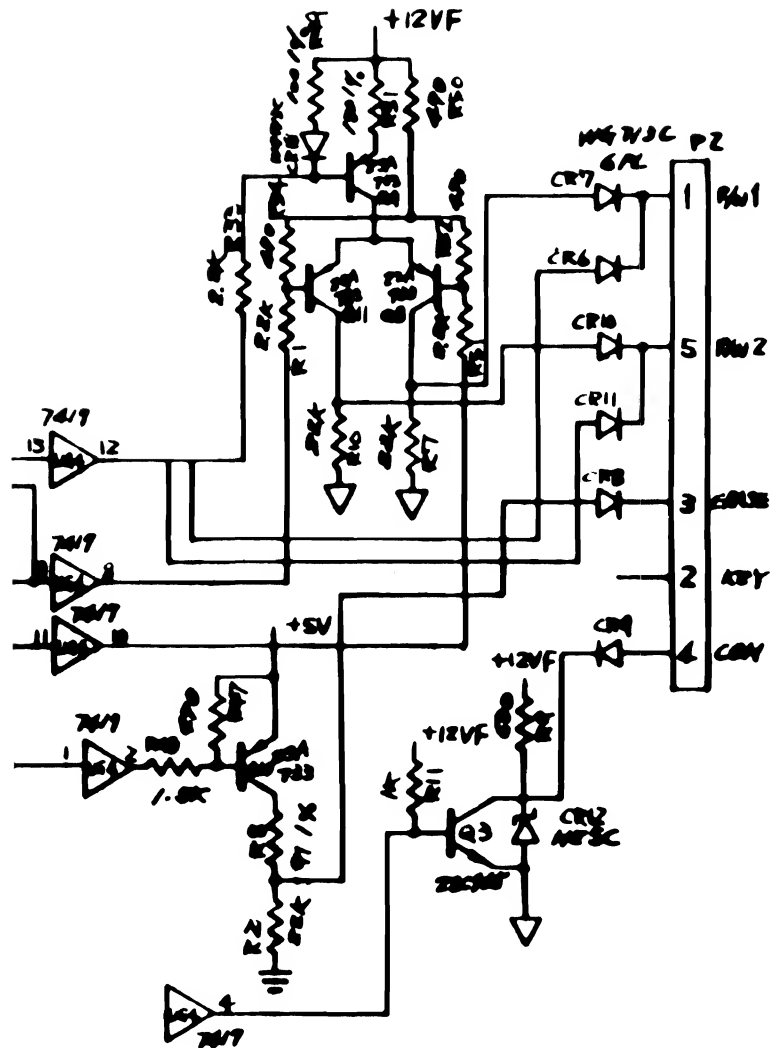


Read Amplifier Circuits

When data is recorded on the disk, a "1" bit is represented on the disk by a change in direction of magnetic flux, caused by a change in direction of current passed through the R/W coil in the R/W head. When a "0" bit is to be recorded, no change in current flow direction occurs, causing the direction of the magnetic flux to remain the same on the disk.



When data is being read from the disk, CEMF is induced into the R/W coil by the magnetic fields on the disk, causing current flow which is detected by the read amplifiers. Current flow through the R/W coil will forward bias either CR6 or CR11, depending on the direction. Q3 and CR9 must be forward biased. The first amplifier, UH7, senses this current flow from the R/W coil on one of the inputs and amplifies it. L8, L9, L10, L11, and C16 act as a low pass filter, suppressing noise on the amplified output. UH5 is a differential amplifier which amplifies the difference of the two input signals from the filter section. UH4 is a peak detector. The output of UH4 will pulse "high" when a "1" is read. This signal is the reconstruction of data recorded. The time domain filter, UG3 times out when a "1" bit has been read, so unwanted "1" bits are not added to the actual data. The one shot, UG3 generates the correct data pulse width so the read/write logic circuits can convert it to parallel for processor control.



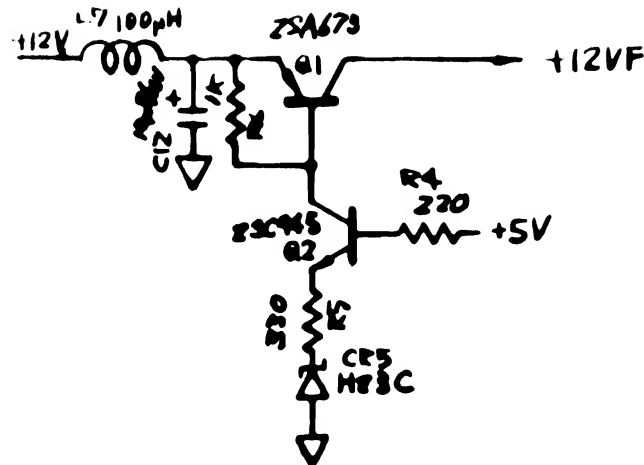
Write Amplifier Circuits

During a write operation, UG4, pin 3, must be "high". This forward biases Q3 and CR9.

If Q₉ of UF6, pin 9, goes "low", Q8 and CR7 become forward biased, passing current flow through R/W 1. If Q₁₀ goes "low", Q11 and CR10 become forward biased, passing current flow through R/W 2.

When a write operation occurs, the ERASE coil is energized by forward biasing Q10. This demagnetizes the outer edges of the track, preventing data on one track from bleeding into the next track.

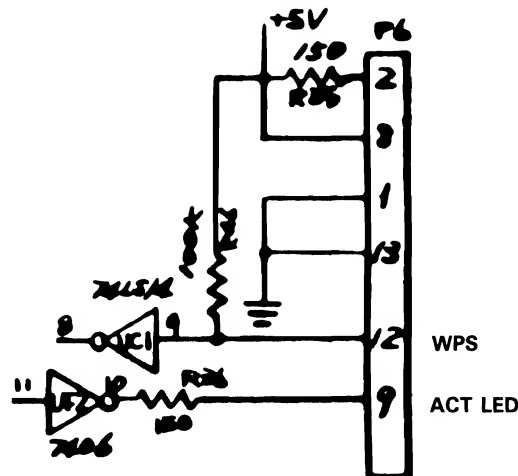
2031 LP CIRCUIT THEORY



Power Up/Down Write Protection

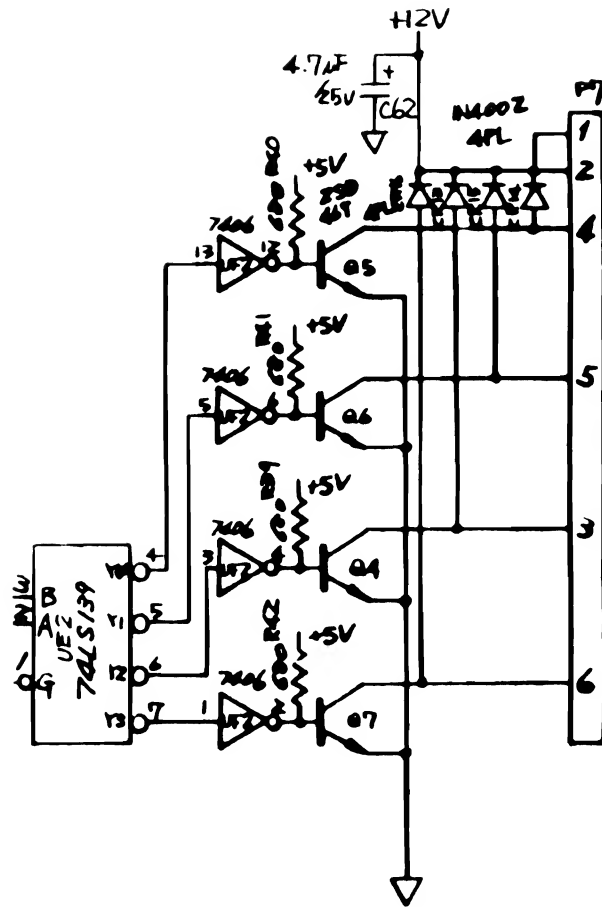
This circuit prevents erroneous data from being written on the disk during power up/down sequences. During a power up, the 12VDC supply is not applied to the R/W coils and amplifier circuits before the processor has control of the logic. During a power down, the 12VDC supply is removed from the R/W coils and amplifier circuits before the processor loses control of the logic.

Q1 acts as a series pass transistor biased to regulate the 12VF output to the R/W coils and amplifier circuits. Q2 is a feedback amplifier monitoring the 5VDC supply. CR5 develops a precise reference voltage for Q2. L7 and C12 delay the 12VDC supply.



Write Protect Switch

Connector P6 connects the control circuits to the W/P switch and activity light. UCD4, a 6522 VIA, monitors the state of the write protect sensor on pin 14 and controls the red activity LED on pin 13.

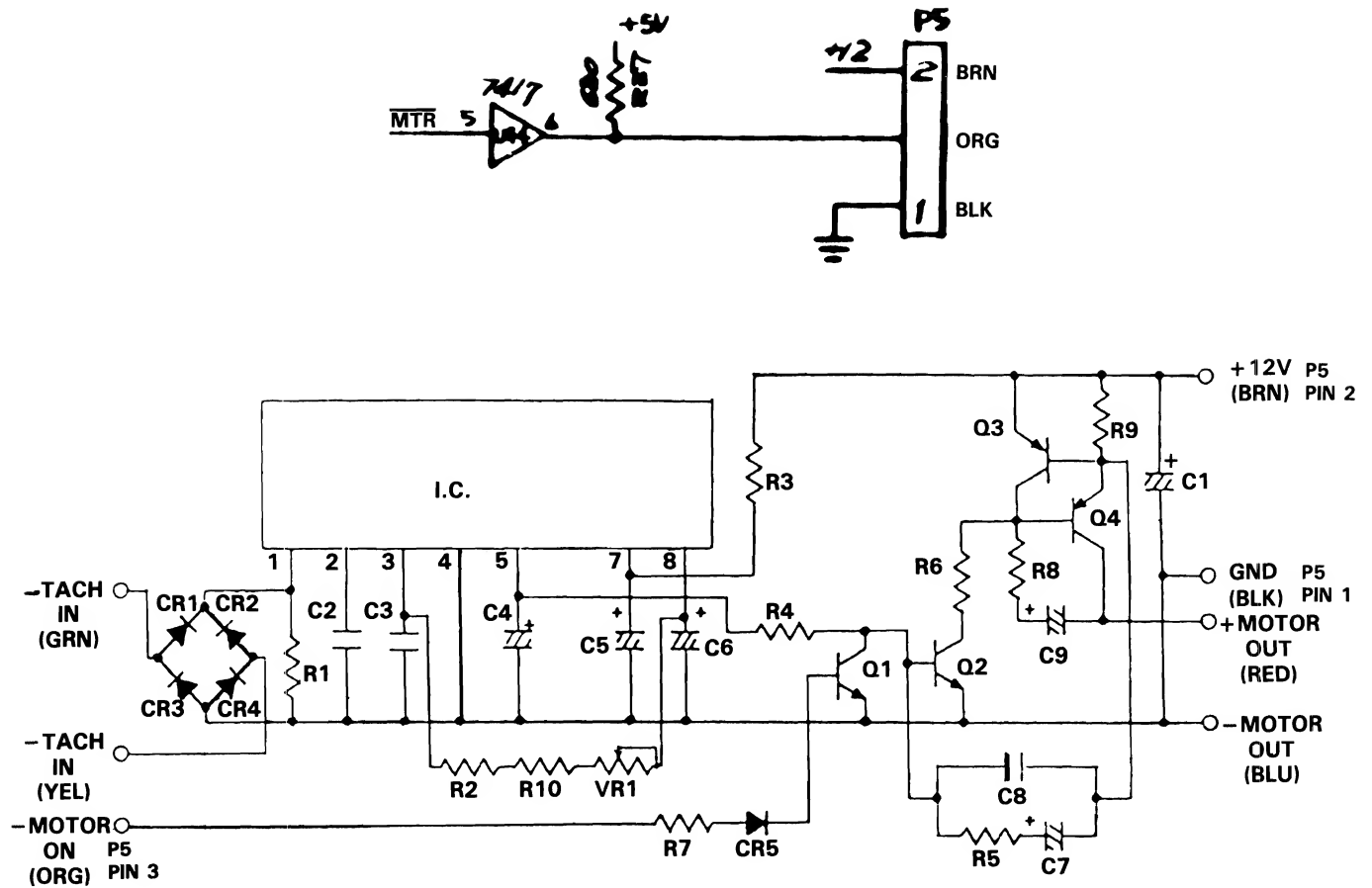


Stepper Motor Control Circuits

The stepper motor is controlled by two outputs on port B of UCD4, the 6522 VIA, STP0 and STP1. These two lines are converted by UE2 to a binary four count to drive the four phases of the stepper motor.

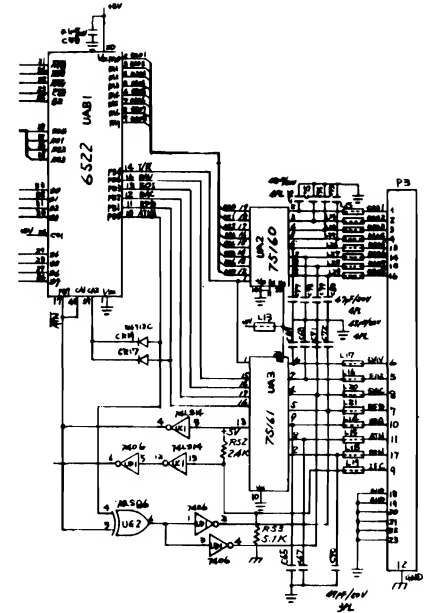
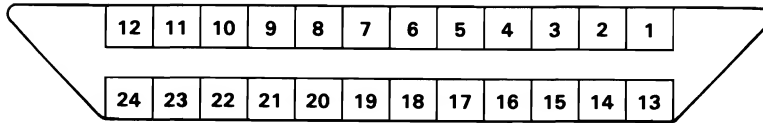
Outputs Y0, Y1, Y2, and Y3 from UE2 are inverted by UF2. The outputs of the inverters drive Q4-Q7. The current output from these transistors drives the individual phase coils in the stepper motor and returns, to the 12VDC supply. CR13-CR16 suppress the CEMF developed by the motor coils.

2031 LP CIRCUIT THEORY



Spindle Motor Control Circuits

MTR output from UF2 pin 8 is passed through current driver UG4 to the motor control PCB. When MTR is "low", Q1 is biased off, and Q2, Q3, and Q4 are biased on, allowing current flow through the spindle motor coil. Attached to the shaft of the spindle motor is an inductive tachometer that generates low level AC voltages, as the motor spins. The output of the tachometer is rectified by CR1-CR4. IC 1 monitors the output of the rectifier and adjusts the bias to Q2, which changes the bias on Q3 and Q4 to regulate motor current for a constant velocity. VR1 is a manual speed adjustment. The speed can be adjusted by watching the 60Hz strobe as the adjustment is made or loading the system test from the diagnostic disk.



IEEE Interface

All of the signals on the interface are controlled by the I/O device UAB1. Eight parallel bi-directional data lines, PA0-PA7, are used as the parallel data bus for the interface. UA2 is an octal bus transceiver used to provide communication on the general purpose interface bus, GPIB, between operating units of the system. The data transfer and bus-management signals are communicated by UA3, thus completing the 16-line interface of the IEEE-488 bus.

DAV	Data Valid	DAV low signifies data is valid on the data bus.
EOI	End or Identify	CBM always sets EOI low while the last data byte is being transferred.
DAC	Data Not Accepted	DAC is low when data is being read and returned high after the last data byte is read.
RFD	Not Ready For Data	RFD is low until all receivers are ready to accept data, then the line will go high.
SRQ	Service Request	Not implemented in BASIC but available to the CBM user.
ATN	Attention	The host sets the signal low while sending commands on the data bus.
REN	Remote Enable	REN is held low by the bus controller and the host has this pin permanently grounded.
IFC	Interface Clear	The host sends its internal reset signal as IFC low to initialize all devices.

PARTS LIST

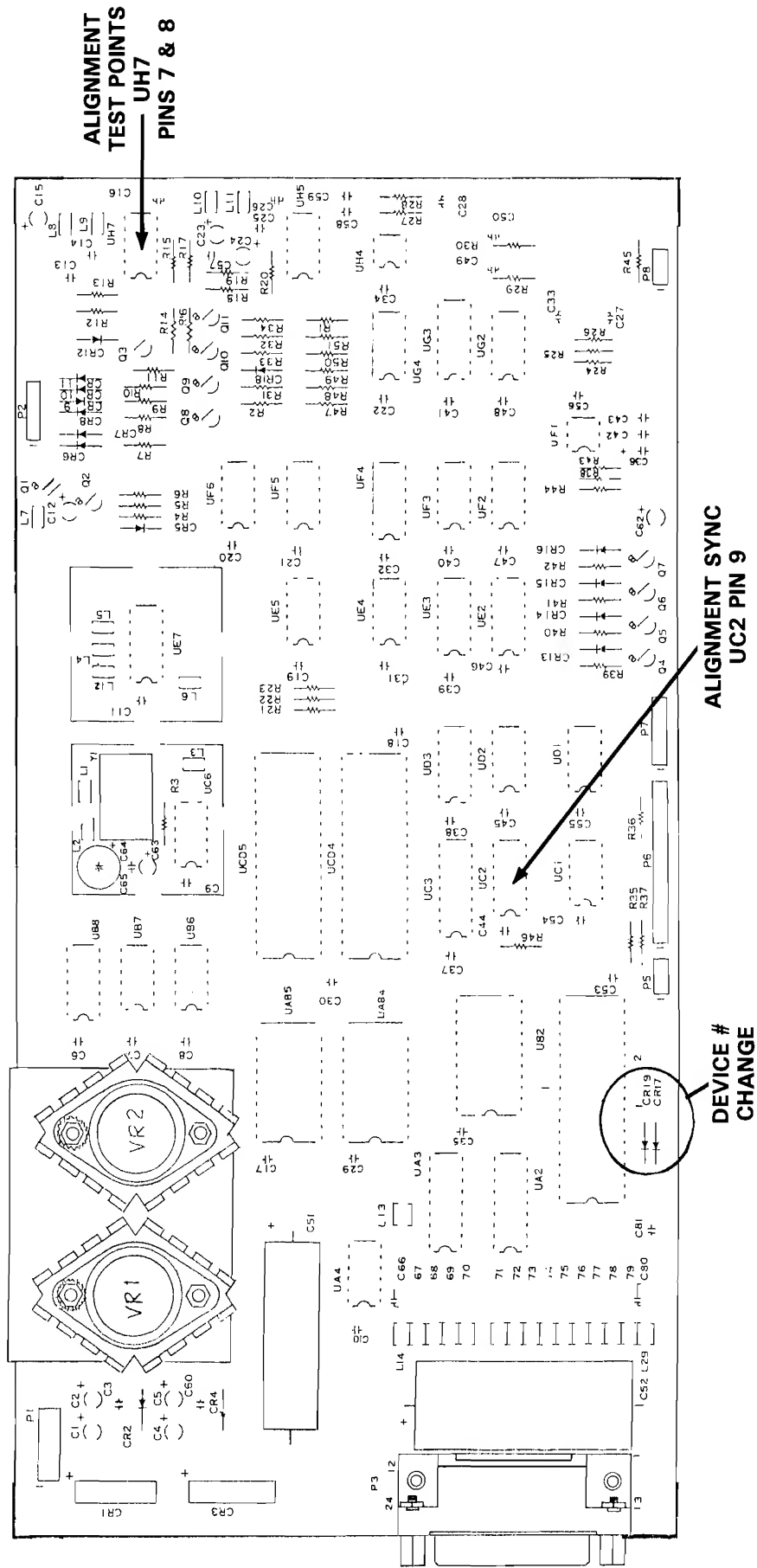
PCB ASSEMBLY #1540033

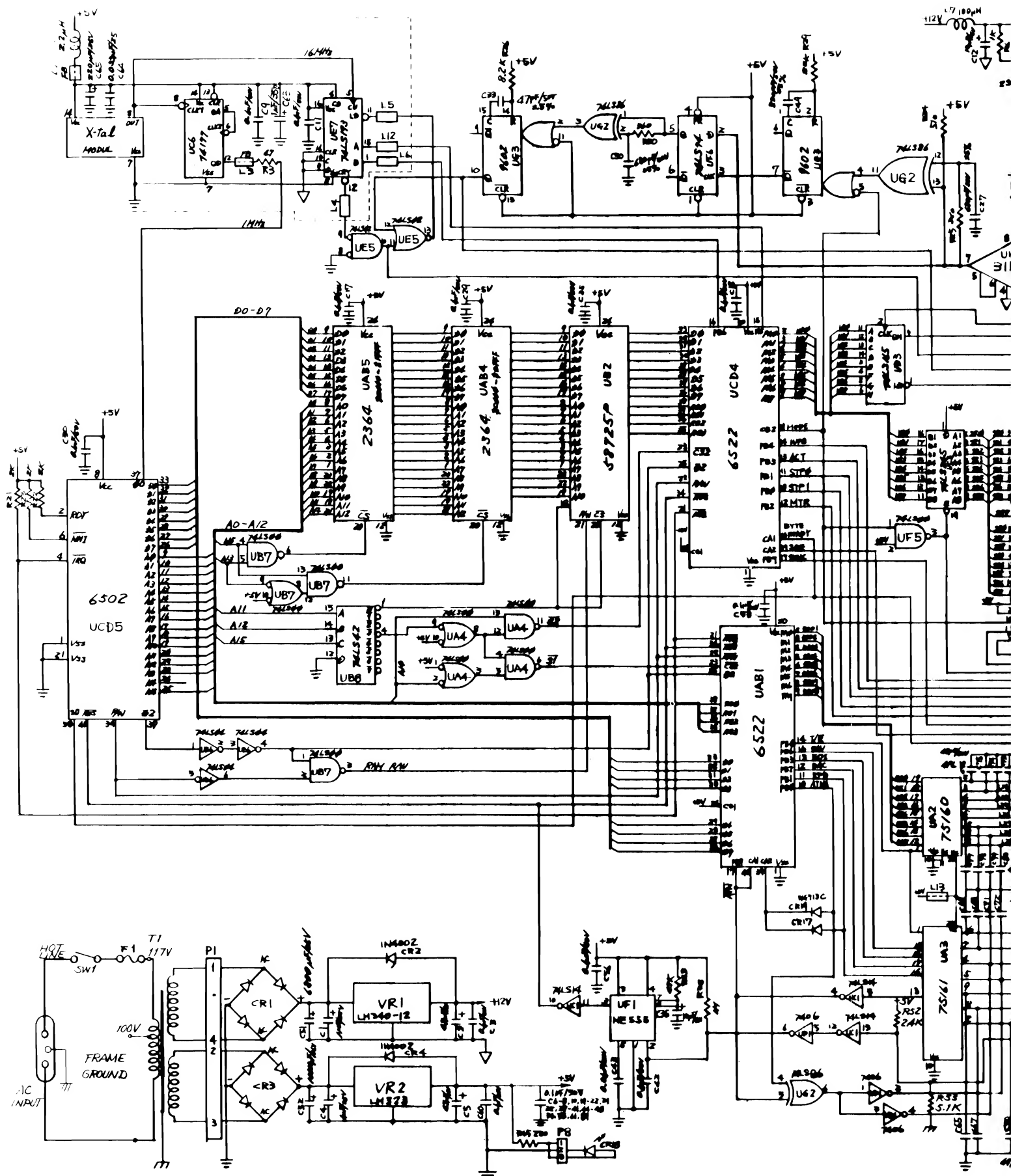
PLEASE NOTE:

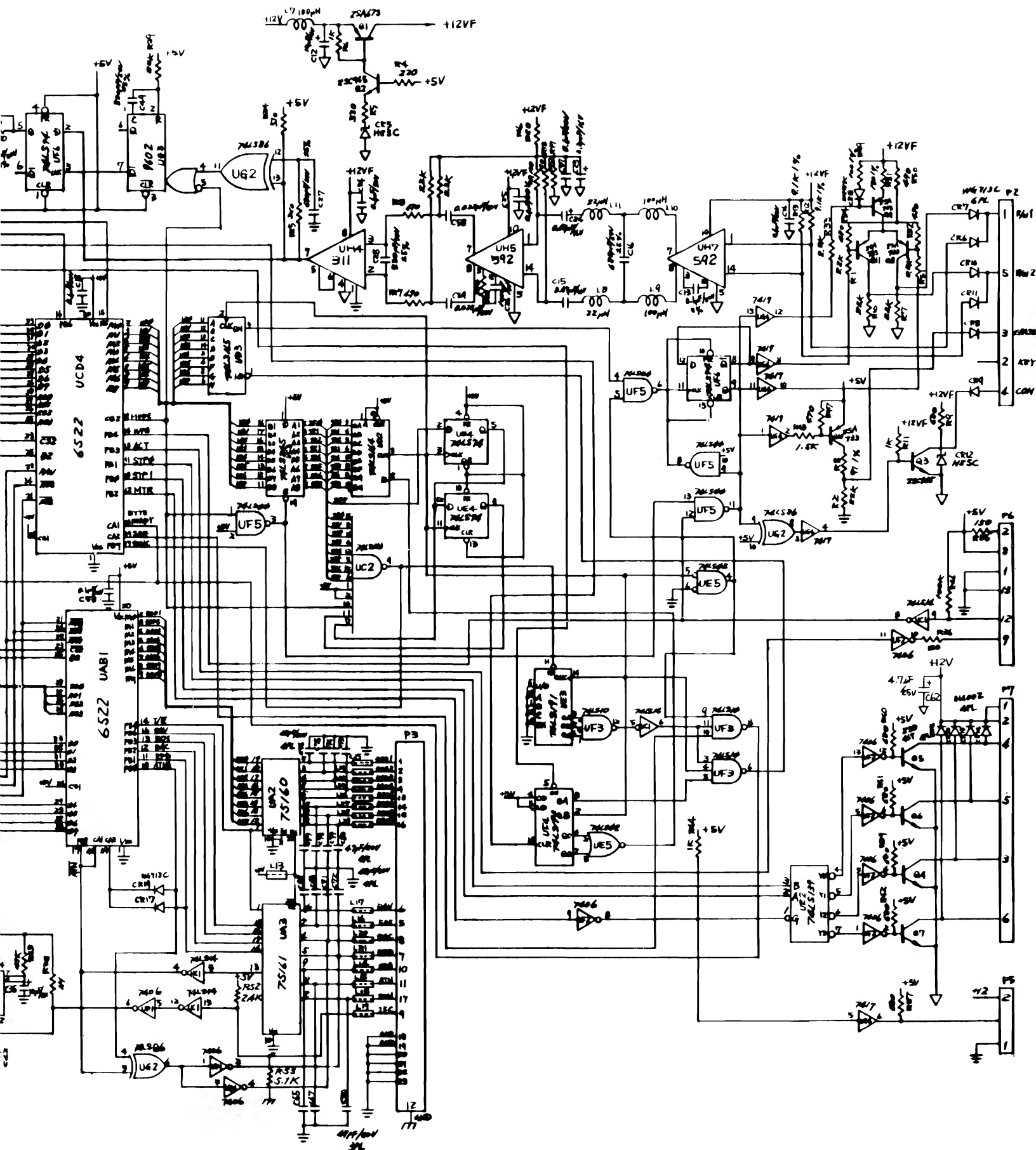
Commodore part numbers are provided for reference only and do not indicate the availability of parts from Commodore. Industry standard parts (Resistors, Capacitors, Connectors) should be secured locally. Approved cross-references for TTL chips, Transistors, etc. are available in manual form through the Service Department, order part #314000-01. Unique or non-standard parts will be stocked by Commodore and are indicated on the parts list by a "C". Vendor Name and part number have been provided for your convenience in ordering custom or unique parts.

INTEGRATED CIRCUITS				RESISTORS (Continued)			
UAB1	6522 VIA	C 901437-01		25	360	R39-42	680
UAB4	ROM \$C000-\$DFFF	C 901484-03		R26	8.2K	R43	47K
UAB5	ROM \$E000-\$FFFF	C 901484-05		R27,28	470	R44	1K
UCD4	6522 VIA	C 901437-01		R29	22K	R45	220
UCD5	6502 CPU	C 901435-01		R30	360	R46	100K
UA2	75160 Transceiver	901493-01		R31	150, 1/4W, 1%	R47	470
UA3	75161 Transceiver	901494-01		R32	470	R48	1.5K
UA4	74LS00	901521-01		R33	2.2K	R49	100, 1/4W, 1%
UB2	TMM2016 RAM	325502-01		R34	470	R50	470
UB6	74LS04	901521-02		R35,36	150	R51	2.2K
UB7	74LS00	901521-01		R37	680	R52	2.4K
UB8	74LS42	901521-17		R38	1M	R53	5.1K
UC1	74LS14	901521-30		CAPACITORS			
UC2	74LS133	901521-15		C1	Electrolytic	1μF, 25V	
UC3	74LS245	901521-45		C2	Elect	47μF, 16V	
UC6	74177	901522-03	Sub:	C3	Ceramic	.1μF, 50V	
	74LS197	901521-54		C4	Electrolytic	1μF, 25V	
UD1	7406	901522-06		C5	Elect	47μF, 16V	
UD2	74LS164	901521-28		C6-11	Ceramic	.1μF, 50V	
UD3	74LS165	901521-12		C12	Tantalum	10μF, 25V	
UE2	74LS139	901521-18		C13,14	Ceramic	.1μF, 50V	
UE3	74LS191	901521-40		C15	Tantalum	.47μF, 16V	+/- 20%
UE4	74LS74	901521-06		C16	Ceramic	680pF, 50V	+/- 5%
UE5	74LS02	901521-21		C17-22	Ceramic	.1μF, 50V	
UE7	74LS193	901521-26		C23	Tantalum	3.3μF, 25V	
UF1	555 Timer	901523-01		C24	Tantalum	.47μF, 16V	+/- 20%
UF2	7406	901522-06		C25	Ceramic	.1μF, 50V	
UF3	74LS10	901521-24		C26	Ceramic	1000pF, 50V	
UF4	74LS193	901521-26		C27	Ceramic	680pF, 50V	+/- 5%
UF5	74LS00	901521-01		C28	Ceramic	330pF, 50V	+/- 5%
UF6	74LS74	901521-06		C29-32	Ceramic	.1μF, 50V	
UG2	74LS86	901521-32		C33	Ceramic	47pF, 50V	
UG3	9602 One Shot	901510-01		C34,35	Ceramic	.1μF, 50V	
UG4	7417	901522-01		C36	Electrolytic	10μF, 16V	
UH4	311 OP AMP	901523-04		C37-42	Ceramic	.1μF, 50V	
UH5	592	901523-08		C43	Ceramic	.01μF, 50V	
UH7	592	901523-08		C44-48	Ceramic	.1μF, 50V	
TRANSISTORS				C49	Ceramic	330pF, 50V	+/- 5%
Q1	2SA673			C50	Ceramic	680pF, 50V	+/- 5%
Q2,3	2SC945 Sub:			C51	Electrolytic	6800μF, 25V	
	2SC1815			C52	Electrolytic	10000μF, 16V	
Q4-7	2SD467 Sub:			C53-57	Ceramic	.1μF, 50V	
	2SC2120			C58,59	Ceramic	.022μF, 50V	
Q8-11	2SA733 Sub:			C60,61	Ceramic	.1μF, 50V	
	2SA1015			C62	Tantalum	4.7μF, 25V	
DIODES				C63	Tantalum	1μF, 35V	
CR1	1.5 A, 50V, Bridge Rectifier			C64	Ceramic	.033μF, 25V	
CR2	1N4002 Signal			C65	Electrolytic	220μF, 25V	
CR3	4 A, 50V, Bridge Rectifier			C66-80	Ceramic	47pF, 50V	
CR4	1N4002 Signal			C81	Ceramic	.1μF, 50V	
CR5	1N5226B, 3.3V, 500mW, Zener Sub:			MISCELLANEOUS			
	HZ3C-2, 3.3V, 500mW, Zener Sub:			P1	Header Assy	Molex # 5271-04A	
	HZ4A-1, 3.3V, 500mW, Zener Sub:			P2	Header Assy	5049-04AG	
CR6-11	1N4148 Signal			P3	Rt Angle Cnnct IEEE	C 903206-01	
CR12	1N5131B, 5.1V, 500mW, Zener			P5	Header Assy	Molex # 3094-03A	
	HZ5C-2, 5.1V, 500mW, Zener			P6	Header Assy	3094-15A	
CR13-16	1N4002 Signal			P7	Header Assy	3094-06A	
CR17-19	1N4148 Signal			P8	Header Assy	3094-03A	
RESISTORS — All Values are in ohms- 1/4 W 5% unless noted otherwise.				L1	Inductor 2.2μH		
R1	2.2K	R10	22K	L2-6	Ferrite Bead		
R2	22K	R11	1K	L7	Inductor 100μH		
R3	47	R12,13	9.1K, 1/4W, 1%	L8	Inductor 22μH		
R4	220	R14,15	2.2K	L9,10	Inductor 100μH		
R5	330	R16,17	220	L11	Inductor 22μH		
R6	1K	R18,19	150	L12-29	Ferrite Bead		
R7	22K	R20	330	VR1	Voltage Regulator, 12V, 1.5A, LM340		
R8	91, 1/4W, 1%	R21-23	2K	VR2	Voltage Regulator, 5V, 3A, LM323		
R9	680	R24	510	Y1	Crystal Module, 16 MHz	C 325566-01	
					Shield Box	4022048-01	
					Shield Cap	4022047-01	

PCB ASSEMBLY #1540033 BOARD LAYOUT



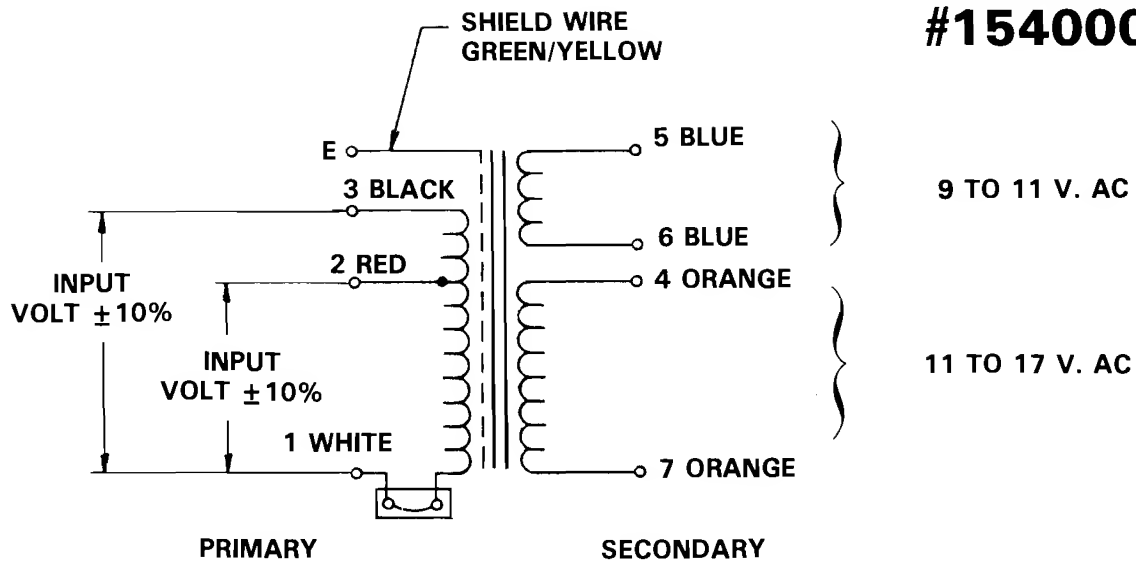




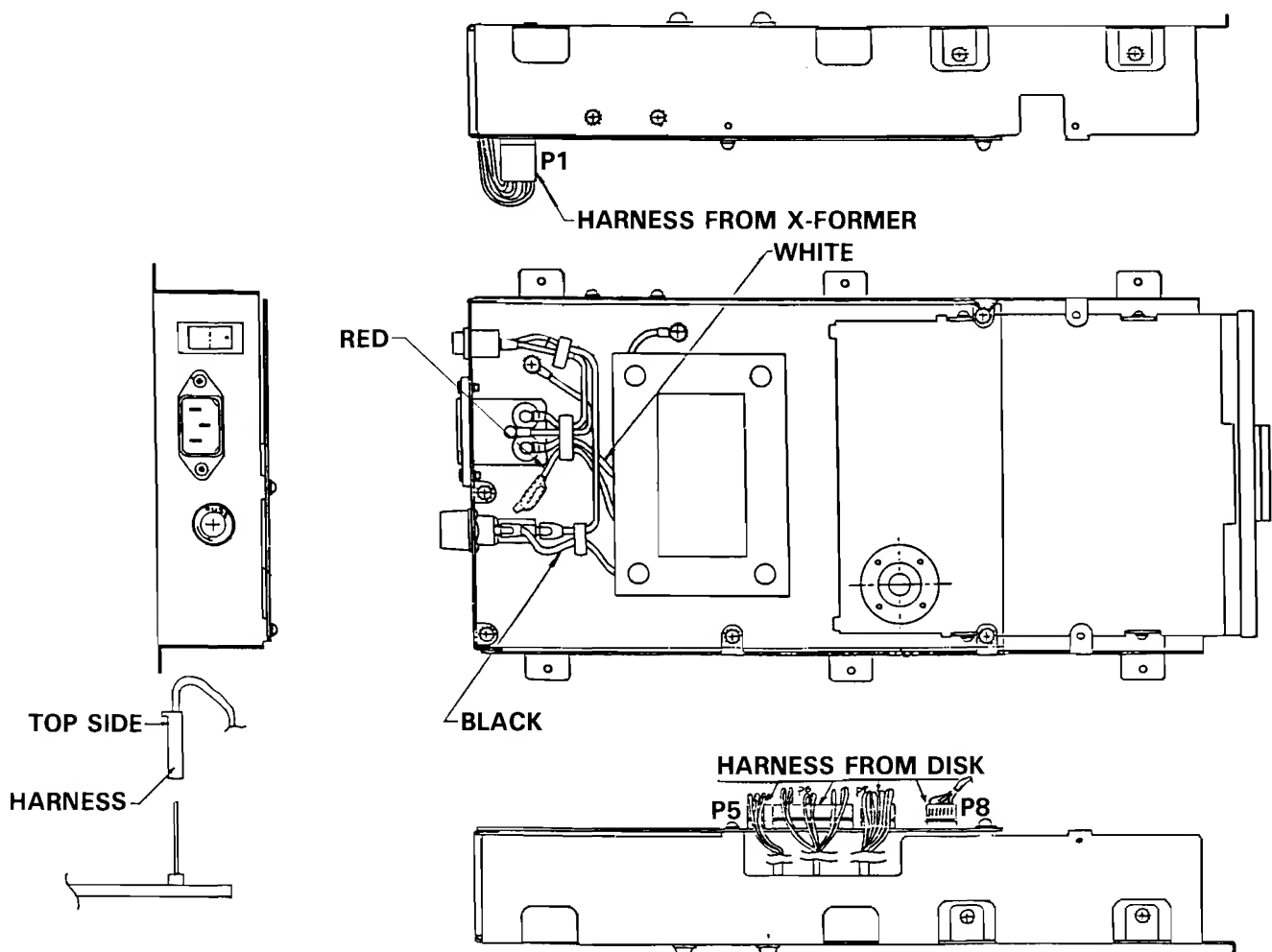
1540/41/2031 LP POWER SUPPLY ASSEMBLY PARTS LIST

FUSE HOLDER	903614-01
ROCKER SWITCH	904509-01
POWER CNNCT FILTER	903467-03 sub:
	325552-01
FUSE, SLOW BLO, 250V, 1.0A	903556-16
POWER TRANSFORMER	1540009-02

2031 LOW PROFILE POWER SUPPLY #1540002-01

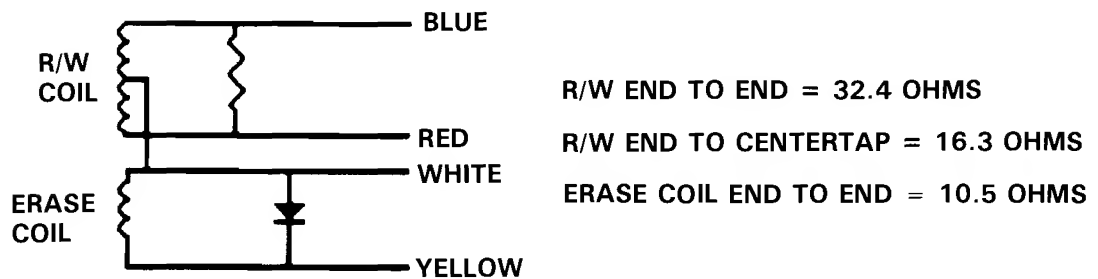
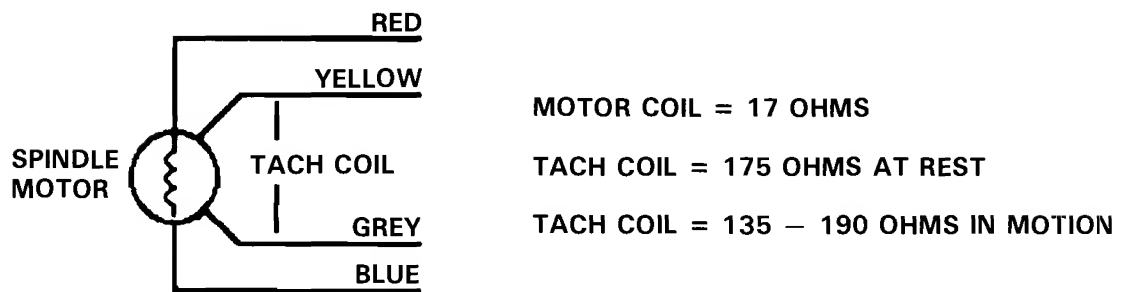
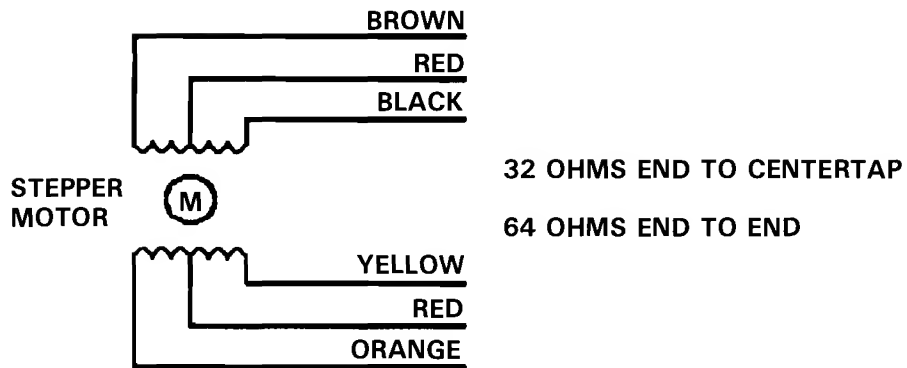


TRANSFORMER



ASSEMBLY DRAWING

RESISTANCE CHECKS LOW PROFILE — ALPS DRIVE



PARTS LIST

32551901 Alps Drive (Black)

32551902 Alps Drive (Brown)

- | | |
|--|---|
| ① 31410001 ALP DOOR/HUB ASSEMBLY
1-Door Assy w/Spring
2-Hub/Collet Assy
3-Arm Support Assy | ⑦ 31410701 ALP MOTOR CONTROL PCB ASSEMBLY
1-Motor Control PCB
2-Harness Assy |
| ② 31410101 ALP LEFT DISK GUIDE ASSEMBLY
1-Diskette Guide
2-LED Assy w/Harness
3-Write Protect Assy | ⑧ 31410801 ALP TENSION PULLEY ASSEMBLY
1-Pulley Wheel w/Spring
2-Plastic Housing |
| ③ 31410201 ALP RIGHT DISK GUIDE | ⑨ 31410901 ALP HOUSING/SPINDLE ASSEMBLY
1-Housing Base
2-Spindle Assy
3-L/R Guide Shafts |
| ④ 31410301 ALP FRONT BEZEL (Black)

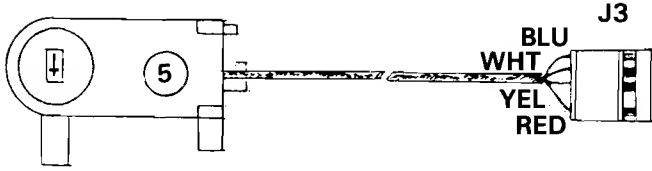
31410302 ALP FRONT BEZEL (Brown) | 31411001 ALP DRIVE BELT |
| ⑤ 31410401 ALP R/W HEAD ASSEMBLY
1-R/W Head
2-Load Arm w/Pad
3-Metal Band

31410501 ALP STEPPER MOTOR ASSEMBLY
1-Stepper Motor w/Harness
2-Stepper Pulley | ⑩ 31411101 ALP EJECT ASSEMBLY
1-Eject Plate
2-Eject Spring

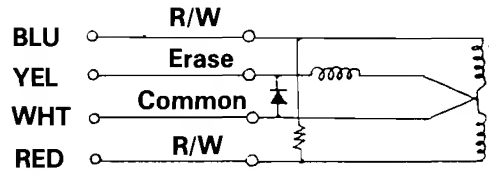
31411201 ALP HARDWARE
1-Assorted Screws
2-Zero Stop Tab

31417401 UNIV Replacement Load Pad |
| ⑥ 31410601 ALP D.C. MOTOR | |

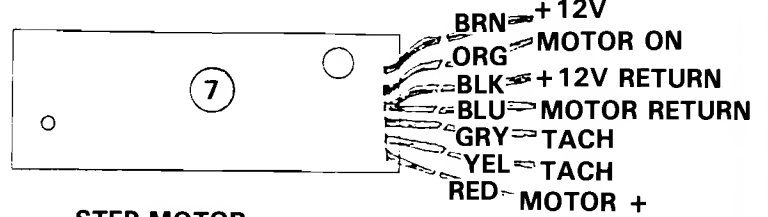
ALPS DRIVE ASSEMBLIES 1540/1541/2031 LP



READ/WRITE HEAD ASSEMBLY



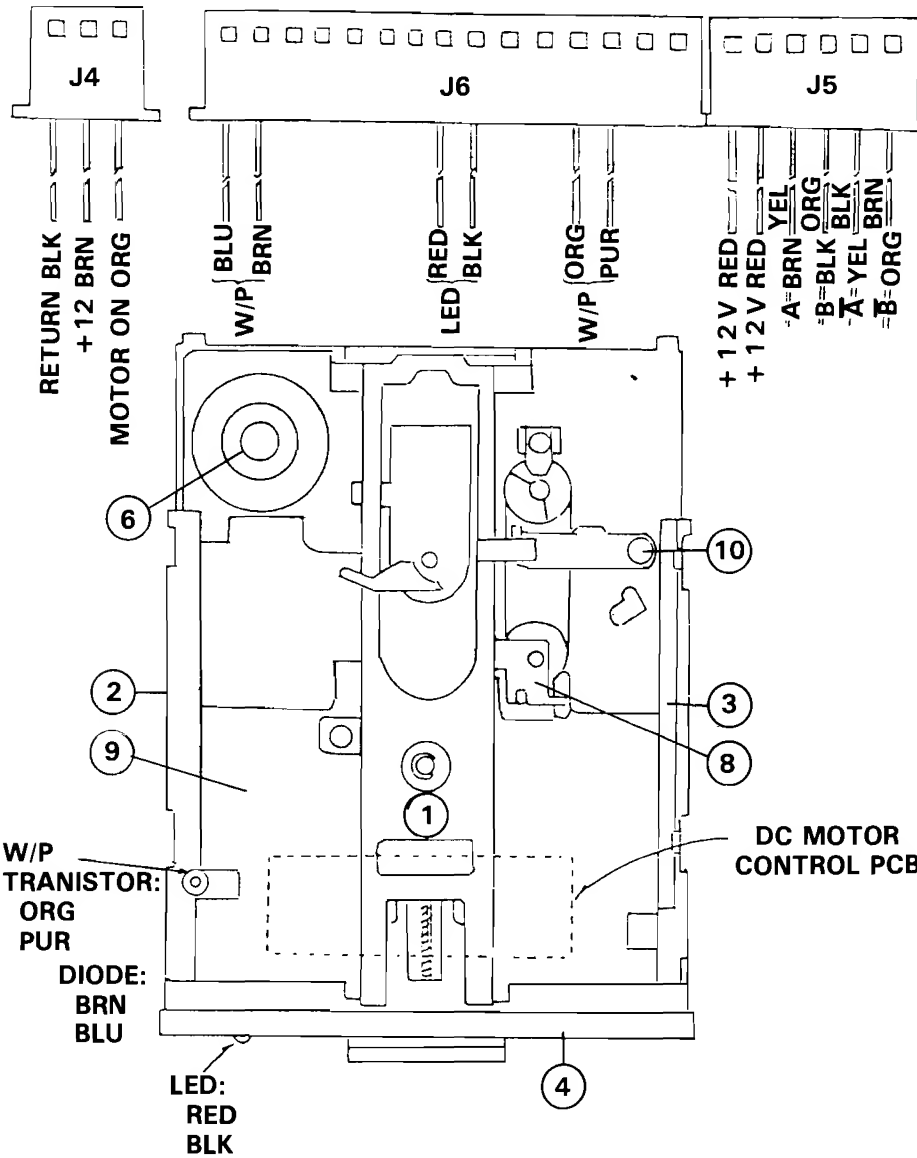
MOTOR CONTROL P.C.B.



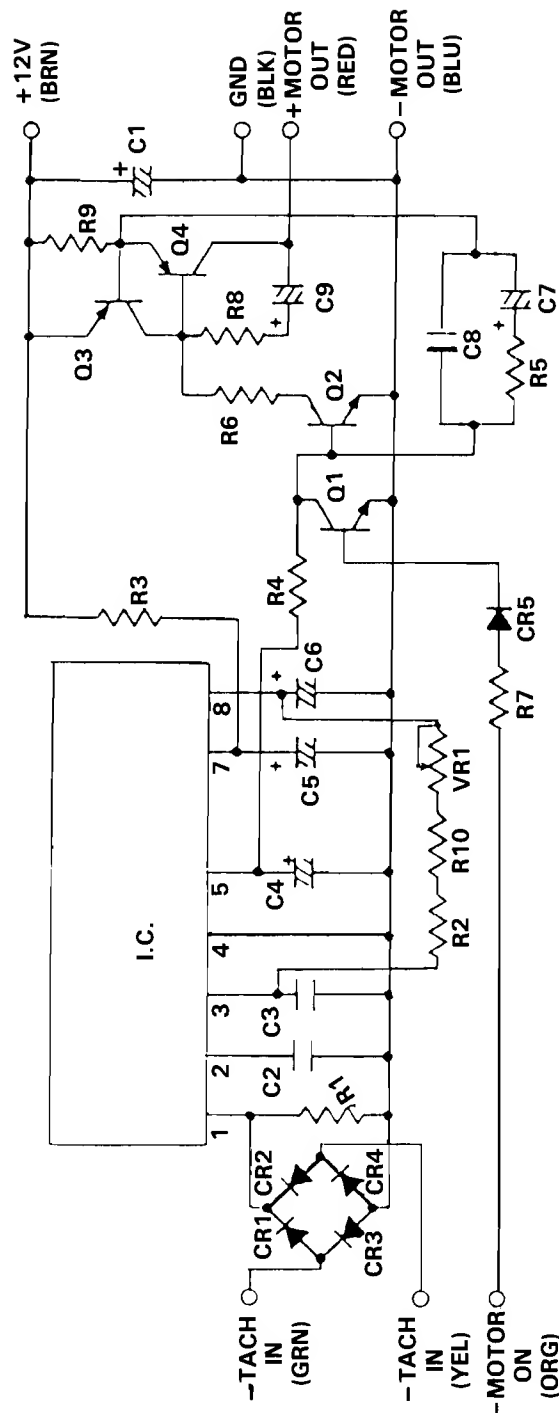
DC MOTOR
CONTROL PCB

FUNCTION

STEP MOTOR



ALPS MOTOR CONTROL BOARD SCHEMATIC



SYMBOL	DESCRIPTION
I.C.	Sony CX-065B
Q1	Transistor 2SC2785
Q2	Transistor 2SC2785
Q3	Transistor 2SA1175
Q4	Transistor B703-Q36E
CR1,2,3,4,5	Diode IN4148
R1,7	Resistor, 1k Ω , 1/4W
R2	Resistor, 68k Ω , 1/4W
R3	Resistor, 220 Ω , 1/4W
R4	Resistor, 3.3k Ω , 1/4W
R5	Resistor, 2.7k Ω , 1/4W
R6	Resistor, 820 Ω , 1/4W
R8	Resistor, 150 Ω , 1/4W
R9	Resistor, 0.68 Ω , 2W
R10	Resistor, 5.1k Ω , 1/8W
VR1	Variable Resistor, 20k Ω
C1,5,6	Capacitor, Electrolytic, 10 μ F, 35V
C2	Capacitor, 0.0047 μ F, 50V
C3	Capacitor, 0.033 μ F, 50V
C4,9	Capacitor, Tantalum, 0.47 μ F, 35V
C7	Capacitor, Tantalum, 2.2 μ F, 16V
C8	Capacitor, 0.068 μ F, 50V

(Fold In)

CITY:

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STREET:

COMPANY:

NAME:

PHONE:

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COMMODORE BUSINESS MACHINES
C-2654
West Chester, PA 19380

Service Documentation

Fold and Tape

DO NOT STAPLE

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